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# DEVELOPMENT AND PERFORMANCE OF PULSE-WIDTH-MODULATED STATIC INVERTER AND CONVERTER MODULES

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16. Abstract

Pulse-width-modulated inverter and converter modules are being developed for modular aerospace electrical power systems. The modules, rated 2.5 kilowatts per module and 10-minute - 150-percent overload, operate from 56 volts dc. The converter module provides two output voltages: a nominal link voltage of 200 volts dc when used with the inverter, and 150 volts dc to a load bus when used separately. The inverter module output is 400-hertz, sinusoidal, three-phase, 120/208 volts. Tests of breadboard models with standard parts and integrated circuits show rated power efficiencies of 71.4 and 85.1 percent and voltage regulation of 5 and 3.1 percent for inverter and converter modules, respectively. Sine-wave output distortion is 0.74 percent.

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# DEVELOPMENT AND PERFORMANCE OF PULSE-WIDTH-MODULATED STATIC INVERTER AND CONVERTER MODULES

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## SUMMARY

Static inverter and converter modules employing high-frequency pulse width modulation are being developed for use in modular aerospace electrical power processing systems. A new concept, staggered-phase carrier cancellation, is used in the inverter to minimize harmonic frequencies and filter weight. The inverter is used in conjunction with a dc-to-dc converter which provides the dc link voltage to the inverter, voltage regulation, current limit, and short-circuit protection.

A dual function of the converter when used independently is to provide dc power at 150 volts to a load bus. The combination of inverter and converter comprises an inverter module for ac systems, and the self-sustaining dc-to-dc converter of this combination when used separately comprises a converter module to power a dc load bus.

Both modules operate from 56 volts dc and are rated for 2.5 kilowatts per module with 150-percent, 10-minute overload capability. Their circuits are compatible with the modular concept and facilitate changing system capacity in 2.5-kilowatt increments. The inverter module provides sinusoidal, 400-hertz, three-phase power at 120/208 volts; and the converter module provides dc power at 150 volts.

Breadboard models were fabricated with state-of-the-art components, integrated circuits, and cage-type construction with plug-in printed circuit cards. Bench tests showed that the new carrier-cancellation concept reduced total harmonic distortion from 105 percent to about 24 percent before filtering. The total harmonic distortion of the 400-hertz sine-wave output voltage is 0.74 percent. Rated power efficiency is 71.4 percent for the inverter module and 85.1 percent for the converter module. Output voltage regulation for +10-percent, -20-percent input voltage variations is 5 percent for the inverter and 3.1 percent for the converter. Experimentation showed that lower-loss filter capacitors will improve performance, and magnetic analysis showed that improved performance can also be realized with lower-loss magnetic cores.

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# INTRODUCTION

The modular concept is intended to provide a "building block" approach to the design of aerospace electrical power-processing systems. Modularization provides flexibility in designing to specified power levels because system capacity can be changed by adding or deleting standardized inverter and converter modules; it can reduce development time and costs since developed and tested off-the-shelf modules can be used; and it should facilitate maintenance through the use of standard replacement modules, particularly in manned missions where such maintenance is feasible. To these ends, a program was initiated to develop the modules for such three-phase, 400-hertz ac systems or for dc power systems. The modules were designed at the Westinghouse Research Laboratories, Pittsburth, Pennsylvania, and the Westinghouse Aerospace Electrical Division, Lima, Ohio, under Contract NAS3-9429. The overall program included development of the basic inverter and converter circuits, automatic paralleling, control and protection circuits, and a visual annunciator circuit to monitor system operation. This report, however, is concerned only with the basic inverter and converter circuits.

Because of previously cited advantages (refs. 1 to 4), high-frequency (9.6-kHz) pulse-width modulation techniques with double-sided modulation are used in both the inverter and converter circuits. Staggered-phase carrier cancellation (ref. 5) is used in the inverter for maximum harmonic attenuation with minimum weight. The basic inverter circuit is a single-phase transformerless inverter which requires a dc link voltage in order to produce an ac output voltage at a higher level than the input dc supply voltage. The dc-to-dc converter which supplies the dc link voltage in this system is a single-ended regulator circuit (ref. 6). And, in addition to providing the dc link voltage, the dc-to-dc converter also provides output voltage regulation and performs the auxiliary functions of startup, current limit, and short-circuit protection. The basic circuits are referred to as submodules; that is, converter submodule and inverter submodule. The nomenclature to describe the combinations of submodules to form converter and inverter modules is illustrated in figure 1.

For the modular system, three of the complete single-phase inverter modules (fig. 1(c)) which are interconnected and controlled through their countdown circuits form a three-phase dc-to-ac inverter module. This is referred to simply as an inverter module (fig. 1(d)). The resulting three-phase output voltage is 120/208 volts at 400 hertz, and the dc link voltage required for this output voltage is a nominal 200 volts dc. This is provided by the dc-to-dc converter from a nominal input voltage of 56 volts dc. The dc-to-dc converter submodule (fig. 1(a)) can operate independently (self-sustaining) of the inverter submodule (fig. 1(b)) and is rated for the same power as the ac inverter stage. Thus, the modular concept can be extended to the formulation of a converter module. This is accomplished from the three dc-to-dc converter submodules used for the single-phase inverter module; they are separately packaged and internally

paralleled to form a dc-to-dc converter module as shown in figure 1(e). The converter submodules also contain the low-voltage supplies for logic circuits and transistor drive power for the inverter and converter submodules. The dc output voltage for the converter modules is 150 volts; this lower voltage is obtained from a tap on the power transformer.

The inverter and converter modules operate from a dc supply of 56 volts nominal and are rated for a continuous power output of 2.5 kilowatts per module. Each has a built-in overload capability of 150 percent of full load for 10 minutes. By circuit standardization the modular concept facilitates changing the power capacity of both ac and dc power-processing systems in 2.5-kilowatt increments merely by adding or deleting additional modules, such as those shown in figures 1(d) and (e), to or from the system.

Two breadboard models of complete inverter modules were fabricated with state-of-the-art components and integrated circuits by the Westinghouse Research Laboratories. The models were tested and evaluated at the Lewis Research Center. As a consequence of the tests, the design was modified. This report presents the results of these tests and includes conclusions, relating to performance and suitability of the power-processing equipment for aerospace applications, which are based on an analysis of the results. Pulse width modulation with staggered-phase carrier cancellation is described graphically and compared with conventional pulse width modulation in appendix A. Detailed descriptions of the developed circuitry are presented in appendix B because this circuitry has only been briefly described previously (ref. 7). Complete circuit drawings and parts lists are contained in appendix C.

## MODULAR DESIGNS

The design goals which formed the guidelines for the development and design of the inverter and converter modules included high reliability, high efficiency, and low weight for space applications. Pulse-width-modulation (PWM) techniques were specified for inverter and converter circuits and the use of low-power integrated circuits was encouraged where applicable. Specific efficiency goals of 81 percent for the inverter module and 90 percent for the converter module were desired.

### Inverter Module

Because the design goals specify high efficiency and low weight, the PWM inverter is designed to operate at a fixed modulation index of approximately 95 percent, as opposed

to a variable modulation index which would provide ac output voltage regulation. Inverter modulation index is defined as

$$M = \left| \frac{T_{on} - \frac{T_c}{2}}{\frac{T_c}{2}} \right| \times 100$$

where $T_c$ is the period of the carrier frequency, $T_{on}$ is the time width of the widest pulse in the PWM pulse train, and M is the modulation index in percent.

The block diagram of the circuitry of the inverter module is shown in figure 2. It consists essentially of three independent, single-phase, pulse-width-modulated inverter circuits and a frequency standard. The $120^{\circ}$ phase separation between phases is produced in the frequency divider.

As stated previously, pulse width modulation with staggered-phase carrier cancellation is used in this design. This technique requires four 9.6-kilohertz carrier frequency phases of rectangular waveform displaced $90^{\circ}$ from each other. These phases are obtained by dividing the 38.4-kilohertz frequency of the crystal oscillator. The 400-hertz sine-wave generator voltage modulates the 9.6-kilohertz rectangular voltages and converts them to pulse-width-modulated voltages of constant amplitude in the PWM logic circuit. Double-sided modulation is used. The PWM signals are amplified in the driver circuit and control the switching of the power transistors in the output circuit, which consists of a double-bridge circuit (i.e., four legs and eight power transistors per phase). Carrier cancellation is accomplished in the output filter circuit (see appendix A). A double bridge is used so that the harmonic frequencies appearing at the output filter are greater than four times the carrier frequency (i.e., 38.4 kHz). This reduces the size and weight of the output filter for an undistorted sine-wave output voltage. The output filter is basically a low-pass inductor-capacitor (L-C) filter with a cutoff at 7800 hertz. Electrolytic capacitors used for dc blocking are selected to series resonate with the filter inductors at 400 hertz to eliminate the filter's inductive reactance effect at 400 hertz. The output filter produces a low resistive internal impedance, which is conducive to parallel operation with other inverter modules.

## Converter Module

The block diagram of the circuitry of a dc-to-dc converter submodule is shown in figure 3. Three such submodules are required for a converter module, as illustrated in figure 1(e). The converter submodule provides a nominal 200 volts dc to the inverter

submodule or 150 volts dc to a dc load bus from the unregulated 56 volts dc input from the supply.

The power stage is a regulated single-ended or flyback-type circuit; a simplified circuit is illustrated within the block (fig. 3). Transformers T1 and T2 are used as chokes for energy storage, for isolation between input and output voltages, and for voltage level setting. Transistors Q1 and Q2 function as switches, applying full voltage to the primary windings during conduction or completely blocking primary current flow when turned off. Transformers T1 and T2 and transistors Q1 and Q2 operate basically in a carrier-cancellation mode; that is, conduction on alternate half cycles (50-percent duty cycle). However, the conduction periods can overlap. When either transistor is conducting, primary current flows, and energy is stored in its transformer. During the nonconducting intervals, the stored energy is delivered to the load. The transistors are switched at a 9.6-kilohertz rate. By varying the ratio of transistor "on" time to "off" time, the output voltage can be varied from zero, when the transistors do not turn on, to a high voltage when the off time is smaller than the on time.

The ratio of the transistor on to off time (duty cycle) is determined in the PWM circuit. This circuit produces double-sided modulation of the pulses and is basically the same as the PWM circuit used for the inverter submodules. But, in this case, the modulation voltage is a controlled dc voltage instead of a 400-hertz sinusoidal voltage. This control voltage is the output of the "OR" gate. The inputs to the OR gate are

(1) ac or dc output sensed voltages for inverter and converter output voltage regulation

(2) Current fault sensing for inverter and converter over-current limit and short-circuit protection

(3) Programmed voltage control during inverter and converter startup

The low-voltage supply provides the voltages to the logic circuits in the inverter and converter circuits and the base drive power to the power transistors in the inverter submodule. The 20-volt supply is disabled during fault conditions and at times during programmed startup. The 9.6-kilohertz oscillator is free running when the converter submodules are used by themselves as a converter module supplying 150 volts to dc loads, and it can be synchronized to the frequency standard when the converter submodules are supplying 200 volts to the inverter submodules in an inverter module.

## Circuit Designs

Specific circuit designs of the functional blocks comprising the inverter and converter submodules are described and discussed in appendix B, and operational waveforms obtained during checkout and tests are included. Complete schematic circuit drawings and parts lists are contained in appendix C.

## Breadboard Fabrication

The circuits as described in appendix B were fabricated into breadboard models for verification tests. Two models were fabricated using standard rack-mounting cabinet enclosures and cage-type construction with printed circuit plug-in boards. Figure 4 shows a complete model. The inverter module was fabricated in three separate phases, with each phase contained in a separate rack-mounted cage. The power semiconductor devices and components in each cage are forced-air cooled with integrally mounted fans. The dc-to-dc converter submodules for the three single-phase inverter modules were also mounted in three separate cages with integrally mounted fans. Each cage is removable and interchangeable with similar cages. Six cages are required for a complete inverter module, and only three cages (i.e., dc-to-dc converter submodules) are required for a converter module. The upper cage and door-mounted light panel contain control and protection circuits and an annunciator circuit, which are not discussed in this report.

Figure 5 is a closeup view of one inverter submodule and one converter submodule cage. It shows the integrated circuits and plug-in printed circuit boards that were used in all the circuits described.

# TEST PROCEDURES

Because the inverter module consists of three independent single-phase inverter modules, the tests for the most part were performed on a single-phase inverter module, as illustrated in figure 6. We believed this procedure would give sufficient data to characterize and evaluate performance. However, a complete inverter module was also run and tested with three-phase loads to check on phase separation and interactions among the phases with balanced and unbalanced loads.

The tests performed included harmonic distortion and frequency spectrum analyses, voltage regulation, regulator gain characteristics, efficiency, transient operation, and individual-circuit operational waveforms. The operational waveforms are included with the circuit diagrams and descriptions in appendix B. The test instruments used are illustrated in figure 6 and include a wave analyzer; oscilloscope and camera; ac voltmeters, ammeters, and wattmeters; dc voltmeters, ammeters, and millivoltmeters; a variable-voltage dc power supply; and variable load banks.

# TEST RESULTS AND DISCUSSION

## Waveform Analysis

The frequency spectrum of the PWM signal voltage output from the modulator circuit is shown in figure 7. This spectrum was obtained for a fixed modulation index of 95 percent and describes a harmonic frequency range extending from 400 hertz, the fundamental, to 50 kilohertz. The harmonic frequencies are shown to cluster in frequency bands which are multiples of the 9.6-kilohertz carrier frequency; that is, approximately 10, 20, 30, 40, and 50 kilohertz. The calculated total harmonic distortion (THD) with respect to the fundamental frequency for this spectrum is 104.7 percent and is calculated from

$$\text{THD (in percent)} = 100 \frac{\sqrt{\sum_{1}^{n} \left| E_n \right|^2}}{E_f^2}$$

where $E_n$ is the rms value of the harmonic frequency voltage and $E_f$ is the rms value of the fundamental frequency voltage. Analysis of this spectrum shows that 90.7 percent of the above total harmonic distortion (104.7 percent) results from harmonic frequencies extending from 8800 to 19 600 hertz as tabulated below:

| Frequency, Hz | Relative amplitude in percent of 400-hertz fundamental voltage $E_f$ |
|---|---|
| 8 800 | 30.0 |
| 9 600 | 72.0 |
| 10 400 | 30.0 |
| 18 800 | 25.0 |
| 19 600 | 25.0 |

The PWM signals from the modulator are used to switch the power transistors in the power circuit, thereby raising their power level. If no harmonic reduction techniques are used, the entire frequency spectrum shown in figure 7 appears at the output filter, but now at a higher power level. This spectrum would require a large filter to produce a low-distortion 400-hertz output because of the large number of low-frequency harmonics present. But the object of the carrier-cancellation technique used in this inverter is to cancel the lower frequency harmonics and present only more easily filtered high-

frequency harmonics to the output filter. Figure 8 shows the spectrum of harmonics at the input of the output filter and illustrates the effectiveness of this cancellation technique. The total harmonic distortion is reduced from 104.7 percent to 24.2 percent by this technique and the first significant harmonics at the output filter (greater than 2 percent) occur at a frequency of 35.6 kilohertz. This harmonic frequency is approximately four times the carrier frequency and is in agreement with the harmonic frequency prediction for the double-bridge power circuit.

The 400-hertz sinusoidal output voltage resulting from filtering the spectrum in figure 8 is shown in figure 9. The rms voltage is 120 volts and this is the line-to-neutral voltage of each phase of the inverter module. The total harmonic distortion of this output voltage waveform is only 0.74 percent as determined from its harmonic frequency spectrum shown in figure 10. And none of the harmonic frequencies contributing to the distortion have a relative magnitude exceeding 0.5 percent of the fundamental frequency voltage.

## Voltage Regulation

dc-to-ac inverter submodule. - Regulation of the single-phase inverter module ac output voltage for unity and 0.7-lagging-power-factor loads as a function of the kilowatt loading is shown in figure 11(a). The percentage of total regulation for +10 percent and -20 percent variations of the 56-volt dc input voltage is 5 percent, where percent regulation is defined by

$$\text{Percent regulation} = \frac{(V_{\text{no load}} - V_{\text{full load}}) \times 100}{V_{\text{full load}}}$$

By appropriate bias level setting, the total regulation can be made equal to $\pm 2\frac{1}{2}$ percent around a nominal 120-volt ac output. The actual regulation of the ac output voltage is performed in the dc-to-dc converter submodule and introduced to the ac power stages through control of the input dc link voltage. Figure 11(b) shows the dc link voltage supplied the inverter submodule for a 0.7-power-factor load. The dc link voltage increases as a function of the load to compensate for the voltage drops in the ac power stage in attempting to maintain the ac output voltage at a constant level.

dc-to-dc converter submodule. - The dc-to-dc converter submodule which supplies the dc link voltage for the dc-to-ac inverter submodule power stages is also the dc-to-dc converter submodule for dc power systems. But for these systems the converter module output voltage is a nominal 150 volts instead of the 200-volt link voltage. The regulation curves of dc output voltage against kilowatt loading for +10 percent and -20 percent volt-

age variations around a nominal 56-volt dc input voltage for the converter submodule are shown in figure 12. The total full-load regulation (833 W) for the converter submodule as defined by these curves is 3.1 percent.

Current limit. - The current limit and short-circuit current protective functions for the inverter and converter modules are performed by the regulator circuit in the converter submodule. It operates to reduce the output voltage when the output load current exceeds a predetermined level. Figure 13 shows both the dc link voltage to the inverter submodule and the ac output voltage as a function of single-phase inverter module load current. The current-limit action (i.e., dc link and ac output voltages decrease) is set to operate when the load current exceeds 17.5 amperes. This set point is approximately 18 percent greater than the full overload current at 0.7 lagging power factor. This set point, however, can be varied over a limited current range. The curves illustrate an overcurrent condition. Under short-circuit conditions, the voltages are reduced to near zero.

Figure 14 shows the current-limit operating region for the dc-to-dc converter submodule supplying a dc load. Current-limit action is set to operate when the current exceeds 8.25 amperes dc. This setting corresponds approximately to the load current when the converter submodule is supplying 150 percent of full-load power rating.

Regulator. - The "dips" in the curves shown in figures 11 and 12 at light loads ($\leqq$250 W) are believed to result from the nonlinearity of the regulator circuit. The duty cycle of the regulator is inversely proportional to the control voltage and in the light-loading region of these curves the regulator is calling for minimum duty cycle with maximum off time of the power transistors. This characteristic is illustrated in figure 15, which shows the control voltage as a function of load current required to maintain the single-phase inverter module output voltage at 120 volts and the converter submodule output voltage at 150 volts. The break point in these characteristics for both the inverter and the converter occurs at a load current of approximately 1.5 amperes. The duty cycle is proportional to load current and therefore adjusts for greater and lesser values around this break point.

The control voltage is obtained from the output of the OR circuit shown in figure 3. The inputs to this OR circuit for steady-state regulations are feedback circuits consisting of operational amplifiers for ac and dc voltage and for current sensing and regulation. These feedback amplifiers provide the required control characteristic shown in figure 15.

An additional compensating voltage is added to the control voltage to compensate for the +10 percent and -20 percent variations in the 56-volt dc input supply voltage. A compensating voltage proportional to the 56-volt input voltage is obtained from the low-voltage supply and is added to the control voltage. (This procedure is discussed in the section on voltage and current regulators in appendix B.) The magnitude of this compensating voltage was sized for proper inverter module output voltage with variations in the

input voltage but was not sized or altered for converter module operation. And this accounts for the displacements of the converter submodule curves shown in figure 12, which were not observed for the single-phase inverter module curves in figure 11. Proper sizing or matching this compensating voltage for converter module operation by means of a separate tap on the transformer in the low-voltage supply should eliminate the displacements of the converter module voltage curves.

## Efficiency

dc-to-ac inverter submodule. - The efficiency curves pertinent to describing the efficiency of the inverter module are shown in figures 16 and 17. Figure 16 considers the efficiency of the inverter submodule and converter submodule power stages individually and in combination with each other when operating into a unity-power-factor load. These curves include only the losses of the power stages and their drivers. Losses of the auxiliary power supplies are accounted for in the overall efficiency curves shown in figure 17.

Figure 16 shows that the efficiency of the ac power stage at rated power is 90.4 percent and the efficiency of the converter submodule supplying the dc link voltage to the ac stage is 85.4 percent. The combined efficiency of both power stages is 77.2 percent. The overall single-phase inverter module efficiency including all losses (fig. 17) is 74.5 percent at rated power and unity power factor, and is 71.4 percent at rated power for a 0.7-lagging-power-factor load. Efficiency variations of less than 1 percent at rated power were observed for dc input voltage variations of +10 percent and -20 percent around the nominal input of 56 volts.

dc-to-dc converter submodule. - The efficiency curve of the dc-to-dc converter submodule supplying power to a dc load at 150 volts is shown in figure 18. The efficiency at the same rated power level (833 W/phase) is 85.1 percent. This compares favorably with the efficiency when it is supplying dc link voltage at 200 volts to the inverter submodule (fig. 16) and is only slightly lower due to higher conduction losses resulting from the lower output voltage at 150 volts dc.

Loss breakdown. - The loss breakdown for the single-phase inverter module operating at an efficiency of 71.4 percent at full rated load and 0.7 power factor is shown in figure 19. The total loss is 335 watts and is distributed as follows:

(1) 140 watts loss in the dc-to-ac inverter submodule

(2) 139 watts loss in the dc-to-dc converter submodule

(3) 56 watts to the low-voltage power supplies

The table also shows that the low-voltage power supplies operate at an overall efficiency at 44.8 percent, that the ac output filter accounts for 58 percent of the total in-

verter submodule loss, and that the core loss of the power transformer in the dc-to-dc converter submodule is 36.6 percent of its total loss. It is believed that the individual losses of these circuits can be reduced through the use of improved components and/or by circuit redesign. For example, a polycarbonate capacitor was tried in the output ac filter during the tests to determine what improvements, if any, would result. A single 125-microfarad polycarbonate capacitor was substituted for four computer-grade, aluminum, electrolytic capacitors normally used. This substitution produced a path for circulating dc currents but did result in an increase in overall single-phase inverter module efficiency of 2.4 percent at rated power with a 0.7 power factor load. At a lighter load of 500 watts, the filter loss was reduced by 33 watts to give a 6.7-percent increase in overall efficiency at this power level. These results therefore indicate that better capacitors with lower loss characteristics should result in improved inverter module performance with higher efficiency.

The cores in the power transformer are C-cores of 2-mil silicon-iron core material, and apparently their loss characteristic at this frequency is not conducive to improving the efficiency. A core material with a lower core loss at this frequency and with a high usable induction range is desired. Possible candidate materials which may result in improved efficiency include supermendur C-cores, laminated 80 percent nickel-iron cores, and powdered permalloy cores. In addition, the primary winding is wound with four conductors in parallel, which possibly could result in excessive circulating currents. A single conductor primary may significantly reduce these losses.

The low-voltage power supply was not originally considered a critical circuit and was designed merely to supply the voltages required for the logic and driver circuits. The results, however, show that the losses and low efficiency of this circuit are significant and contribute to a lower overall single-phase inverter module efficiency. A redesign of the power supply circuit with more emphasis placed on optimizing its performance should contribute to raising the overall efficiency.

## Transient Operation

Single-phase inverter module load switching. - The single-phase inverter module was tested for step-load changes of 0 to 50, 0 to 100, 0 to 150 percent FL (full load) and load power factors of 0.7 lagging and 1.0. The average turnon and turnoff characteristics for complete recovery of these transient conditions were found to be 115 milliseconds for turnon and 230 milliseconds for turnoff. A typical transient response curve is shown in figure 20. The test conditions for this transient were a step load change of 0.7-power-factor load from 0 to 100 percent FL. The turnon time is 110 milliseconds and the turnoff time is 240 milliseconds.

The transient response trace in figure 20 shows an initial dip in ac volts (Vac) as ac current (Iac) builds up, followed by an overshoot and damped oscillations in both Vac and Iac as the current turns on. The initial voltage dip is caused by a partial discharge of the output capacitor of the dc-to-dc converter submodule to supply this load current (reference capacitor C in fig. 3 and also converter submodule schematic diagram in appendix C) and the oscillations occur due to a readjustment of the duty cycle of the power stage in the converter submodule from duty cycle 1 for Vac = 120 volts at Iac = 0 to duty cycle 2 for Vac = 120 volts at Iac = full load current. At turnoff, Iac goes to zero instantly but the inherent time lag in the regulator prevents a rapid change in duty cycle from duty cycle 2 to duty cycle 1, consequently Vac spikes at this instant. But the recovery time during turnoff is limited primarily by the discharge ramp of the output filter capacitor in the dc-to-dc converter submodule. This is a 470-microfarad capacitor and accounts for the long discharge time.

Short-circuit response. - The short-circuit response of the single-phase inverter module is illustrated in figure 21. Prior to step 1, the single-phase inverter module is supplying a load current of 9.92 amperes to a full rated load at 0.7 lagging power factor and the output voltage is 120 volts. At step 1, the short circuit is applied and the immediate corrective action is to disable the 20-volt supply. This removes all the drive to the power transistors and both the load current and output voltage go to zero as shown. The single-phase inverter module remains at the zero output condition for 380 milliseconds before the startup sequence commences at step 2. At startup the 20-volt supply is enabled, the control voltage is clamped at its maximum value, and the converter submodule output filter capacitor is allowed to discharge. During this sequence the modulation gate is turned off so that the output voltage is nearly zero, but the discharge of the capacitor allows a current surge to the load as shown. During the time interval between steps 2 and 3, the modulation gate is turned on approximately 200 milliseconds after the capacitor discharges. After an additional 200 milliseconds delay, the control voltage is unclamped from the startup circuit and its control is taken over by the current-limit circuit.

At step 3 the conditions existing are that the 20-volt supply is enabled, the modulation gate is on, and the current-limit circuit is controlling the regulator control voltage and consequently the output current and voltage. The current builds up in accordance with a programmed ramp function, as shown, which limits the capacitor charging current. The current between steps 3 and 4 is limited to approximately 18 amperes by the current-limit circuit with the short circuit still applied, and the output voltage is less than 5 volts during this interval. The total elapsed time between the application of the short circuit at step 1 and the current buildup to its current-limit value at step 3 is 1100 milliseconds.

At step 4 the short circuit is removed. The current readjusts to its full-load condition of 9.92 amperes and the voltage builds up to its rated output of 120 volts. The recovery time after removal of the short circuit is 120 milliseconds.

## Three-Phase Operation of Inverter Module

The three single-phase inverter modules were interconnected to operate as a three-phase dc-to-ac inverter module. The testing was not extensive but rather its performance was checked to determine whether it did operate as a three-phase inverter module and whether it exhibited any marked deviations from its performance as individual single-phase inverter modules.

Tests were run with both balanced and unbalanced loads ranging from zero to full load in various combinations among the phases. The results showed satisfactory three-phase operation with respect to $120^{\circ}$ phase separation among phases and maintenance of balanced phase voltages with unbalanced loading conditions. No interaction among phases under load conditions and no marked deviations were observed. The three-phase output voltages for a balanced full-load condition are shown in figure 22.

# SUMMARY OF RESULTS

For use in a modular approach to power processing for space power systems, both dc-to-ac inverter modules and dc-to-dc converter modules were designed. The dc-to-dc and dc-to-ac stages were packaged separately and can be used individually or in combination. In particular, three dc-to-ac systems were used in combination to supply three-phase ac power. In each case the modules are self-protected and provide both output voltage regulation and overcurrent protection.

Breadboard models were built and tested. The following results were obtained:

1. The staggered-phase carrier-cancellation technique with double-sided pulse width modulation (PWM) reduced total harmonic distortion of the PWM waveform from 104.7 percent at the output of the modulator to 24.2 percent at the input to the ac filter circuit. The first harmonic frequencies presented to the filter occurred at four times the carrier frequency, or 38.4 kilohertz.

2. The dc-to-ac inverter submodule operated independently as a 400-hertz single-phase inverter providing 833 watts of output power with a power factor of 0.7 and having a 150-percent overload capability for 10 minutes. Three such inverter submodules were interconnected as a three-phase inverter module producing 2.5 kilowatts at 0.7 power factor (PF) and having a 150-percent overload capability for 10 minutes.

3. Measured performance characteristics of the inverter submodules are as follows:

a. The output voltage is 120 volts, line to neutral, 400 hertz sinusoidal with a total harmonic distortion of 0.74 percent.

b. Total ac output voltage regulation is 5 percent for dc input voltage variations of +10 percent and -20 percent.

c. Full load efficiency at 0.7 PF is 71.4 percent.

d. Average transient recovery times for load switching are 115 milliseconds turnon and 230 milliseconds turnoff.

e. Overload and short-circuit currents are limited to approximately 18 percent greater than the full overload current rating at 0.7 PF. Average short-circuit recovery time to current-limit operation is 1100 milliseconds.

4. Measured performance characteristics of the converter submodules are as follows:

a. The output voltage is 150 volts dc.

b. Total dc output voltage regulation is 3.1 percent for dc input voltage variations of +10 percent and -20 percent.

c. Full load efficiency at 150 volts dc is 85.1 percent.

5. Major losses in the inverter and converter are in the power transformer in the converter, in the capacitors in the inverter's ac output filter, and in the low-voltage supply for the logic and drive circuits. It appears that these losses might be reduced through circuit redesign and through selection of capacitors and magnetic cores having inherently lower losses.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, April 23, 1971,
120-60.

# APPENDIX A

# GRAPHICAL COMPARISON OF CONVENTIONAL AND CARRIER-CANCELLATION PULSE WIDTH MODULATION

## Conventional Pulse Width Modulation

The single-bridge circuit shown in figure 23 can be used for both conventional pulse width modulation and the carrier-cancellation PWM technique. It consists of the power transistors Q1 to Q4, drive transformers T1 and T2, filter elements L and C, load, and the single-source dc supply voltage connected across the bridge. The secondary windings of the drive transformers are connected such that only one of the two transistors forming a leg of the bridge is conducting at a given time.

The PWM signal voltages are applied to the primary windings of the drive transformers; and the voltages appearing at the nodes, $V_P$ and $V_Q$, are identical to their primary voltages but at higher power levels. They contain both the square-wave carrier frequency and the low-frequency modulation voltages. The voltages at nodes $V_x$ and $V_y$, however, contain only the average values of the low-frequency modulation since the high-frequency components have been attenuated by the filter components L and C. The load voltage is the difference between $V_x$ and $V_y$; that is, $V_L = V_x - V_y$ and is proportional to $V_P - V_Q$. The voltage waveforms for zero modulation are shown in figure 24(a). Traces 1 and 2 are the unmodulated square-wave carrier frequency voltages at nodes $V_P$ and $V_Q$. These traces are similar to the voltages applied to the primary windings of T1 and T2. The carrier frequency is 9.6 kilohertz and is the same as the carrier frequency of the PWM inverter described in the text of this report. The output voltage $V_L$ is shown in trace 3. It is a square wave of the same frequency but of double amplitude since $V_P$ and $V_Q$ are 180° out of phase and $V_L = k(V_P - V_Q)$, where k is a proportionality constant.

The voltage waveforms for a modulation index approaching 100 percent are shown in figure 24(b). Modulation index is defined as

$$M = \left| \frac{T_{on} - \frac{T_c}{2}}{\frac{T_c}{2}} \right| \times 100$$

where $T_c$ is the period of the carrier frequency in seconds and $T_{on}$ is the width in seconds of the widest pulse in the PWM pulse train. The widest pulses in trace 2 of fig-

ure 24(b) are shown as symmetrical around $\pi/2$, and for 100-percent modulation index their widths should be equal to $T_c$. But the existence of the extremely narrow pulse at $\pi/2$ represents a practical limitation imposed by the finite switching characteristics of transistors toward achieving a 100-percent modulation index. The width of this pulse is determined by the turnon and turnoff switching speeds; and with practical devices, modulation indexes from 90 to 95 percent are attainable with high-speed transistors switching on the order of 1 microsecond.

Traces 1 and 3 of figure 24(b) illustrate the means of generating the double-sided pulse-width-modulated pulse trains in traces 2 and 4. The triangular wave is obtained by integrating the square-wave carrier voltage, and the sine-wave voltage is the modulation voltage. The triangular voltage and the sine-wave voltage are compared in a voltage level detector circuit which is at positive saturation when $V_{triangle} > V_{sine}$ and is at negative saturation when $V_{triangle} < V_{sine}$. These characteristics produce a pulse train of constant amplitude, and the pulse widths are determined by the intersections of the triangular and sine-wave voltages. The intersecting points in traces 1 and 3 are projected onto the time axes in traces 2 and 4 to determine the pulse widths. The sine-wave modulating voltages are phased such as to produce positive-going modulation in trace 2 and negative-going modulation in trace 4.

The power PWM pulses at nodes $V_P$ and $V_Q$ are shown in traces 2 and 4 and their difference is shown in trace 5. The frequency of the pulses in trace 5 are the same as the carrier frequency so that conventional pulse width modulation provides no carrier cancellation and no advantages to reduce filter weight and size. The filtered ac output voltage across the load at $V_x$ and $V_y$ is the dotted half-sine wave shown in trace 5. The frequency of the sine-wave output voltage is 400 hertz, the same as the frequency of the modulating voltage.

## Carrier-Cancellation Pulse Width Modulation

Single-bridge circuit. - The same bridge circuit shown in figure 23 for conventional pulse width modulation is used for carrier-cancellation pulse width modulation in a single-bridge circuit. But the carrier voltages applied to each transformer (T1 and T2) and to each leg of the bridge are in phase with each other. The voltage waveforms for zero modulation are shown in figure 25(a). Traces 1 and 2 are the in-phase carrier frequency power pulses of equal amplitudes at nodes $V_P$ and $V_Q$. The output voltage at zero modulation is zero as shown in trace 3 because $V_L = k(V_P - V_Q)$ and $V_P = V_Q$.

The voltage waveforms for 100-percent modulation index are shown in figure 25(b). Formulation of the PWM pulse trains, traces 1 and 3, are the same as for conventional pulse width modulation; and the PWM power pulse trains at nodes $V_P$ and $V_Q$ are

shown in traces 2 and 4. The significant difference, however, is illustrated in trace 5, which is a trace of $V_P - V_Q$ and is proportional to the output voltage. The period $T_H$ of this output pulse train is one-half the period of the carrier voltage $T_c$, and $f_H = 2f_c$. The carrier frequency, therefore, has been cancelled and the high-frequency harmonics of this pulse train presented to the output filter occur at frequencies equal to and greater than $2f_c$. The higher frequency harmonic components can be filtered out with a smaller filter than if lower frequency harmonics were present, so that the smaller filter presents a size and weight reduction. The sine-wave output voltage of this pulse train is the dotted half-sine wave shown in trace 5.

Double-bridge circuit. - The double-bridge circuit used for staggered-phase carrier cancellation is shown in figure 26. This circuit uses eight power transistors and the secondary windings of the four drive transformers are connected such that only one transistor per leg is conducting at a given time. The voltage nodes are $V_P$, $V_Q$, $V_R$, and $V_S$. The output voltage $V_L$ equals $V_x - V_y$ and is proportional to $(V_P + V_R) - (V_Q + V_S)$.

The double-bridge circuit requires four carrier frequency channels for its operation, with each channel phase shifted by $90^{\circ}$ from the adjacent channel. These channels are illustrated in figure 27, which shows the voltage waveforms for a 100-percent modulation index. A few cycles for each of the carrier frequency channels are shown in traces 1 and 4. The frequency of each square-wave channel is 9.6 kilohertz and each channel is displaced by $90^{\circ}$ from the next channel as shown. Construction of the PWM pulse trains for each leg of the bridge is illustrated in traces 5 to 8 and use the same technique as previously described. And the resulting PWM power pulse trains at the node points in each leg of the bridge are shown in traces 9 to 12. The output pulse train is shown in trace 13 and was constructed from the relation $V_L = k(V_P + V_R) - (V_Q + V_S)$ by summing the individual pulse train voltages at each break point along the time axis. Trace 13 shows that four high-frequency pulses are contained within the time span $T_c$, so that $\tau_H = \tau_c/4$ and $f_H = 4f_c$. The staggered-phase carrier-cancellation technique therefore cancels not only the carrier frequency, but, with the exception of the fundamental modulating frequency, all harmonic frequencies up to four times the carrier frequency. And the harmonic frequencies at the output filter are greater than $4f_c$. The dotted half-sine wave represents the 400-hertz output voltage of this PWM signal after filtering.

Figure 27(e) is a scope trace photograph obtained by summing the four outputs of the pulse width modulator circuits of the experimental inverter. It is in close agreement with trace 13, which was obtained graphically.

# APPENDIX B

## CIRCUIT DESCRIPTIONS

### Principles of Operation

Inverter system. - A single phase of the staggered-phase carrier-cancellation PWM inverter is in reality four identical and independent inverters sharing a common frequency reference, divider circuit, and power supply. Their four outputs are added together at the last stage of the inverter in a series parallel arrangement such that the low-frequency harmonics, up to the fourth harmonic of the carrier, tend to cancel.

The common power supply in figure 28 is the dc-to-dc converter supplying a nominal 200 volts to the inverter. The frequency reference circuit is a stable oscillator which determines the frequency of the carrier and modulation waves. The countdown circuit generates four $90^{\circ}$-phase-displaced 9.6-kilohertz square waves, which become the carriers; and 400-hertz waves, which are used to form the modulation wave after passing through the 400-hertz sine-wave generator.

The outputs of the countdown circuit are square waves, so each of the four carrier phases of the inverter has an integrator to convert the carrier into a triangle wave suitable for modulating. The integrated carrier is combined with the reference 400-hertz sine wave in each modulator to form one of the four PWM staggered-phase signals. The driver boosts the power level sufficiently to drive the bases of the two power stage transistors in each phase. The bridge outputs pass through series L-C filters and are added to the other bridge filter outputs at the load.

dc-to-dc converter. - The dc-to-dc converter (fig. 29) contains many of the same compopents as the inverter, except the converter has only two phases, which are independent. The frequency reference and countdown circuits are replaced by a 9.6-kilohertz two-phase multivibrator, which may be either free-running or synchronized from the inverter frequency reference. The two $180^{\circ}$-phase-displaced outputs of the multivibrator are integrated, modulated, boosted in the driver, and stepped up in the output stage. The outputs are added at the rectifier outputs and applied to a common filter. The modulating signal in this case though is a dc level, which determines the converter and inverter output voltages.

Control system. - The control and regulation system controls the system in three ways: (1) the 20-volt supply, which is necessary for any power stage operation; (2) the modulation gate, which affects only the inverter; and (3) the dc-to-dc converter control or modulation voltage, which controls the converter output. The various blocks of the control system are shown in figure 30. The elements in the upper left are concerned with startup and restart of the system. There are two sequences, depending on whether the

output of the inverter is 120 volts or zero at the time of startup. The elements in the upper right control the linear operation of the converter. These four regulators are OR'd together so that any regulator can override the others to reduce the output. The control system has six sensors which detect the converter and inverter output voltages and currents and the input voltage.

## Circuit Descriptions

The diagrams mentioned in this section are simplified drawings; the complete circuit is shown in appendix C. Operational amplifier frequency compensation and all integrated circuit (IC) power supply connections are eliminated, as are many noise suppression capacitors and redundant parts. Each IC function has a separate part number, and a gate with an expander is shown as a single gate with as many inputs as required.

All the digital IC's are Westinghouse DTL, passive pullup, and are connected between the +6-volt supply and ground. The operational amplifiers are Westinghouse type WS 161Q. They have relatively low gain and output swing, but have a Darlington input for low input bias current. They are operated from the ±12-volt supplies.

Inverter system. - The inverter system consists of the frequency reference circuit, the countdown circuits, the 400-hertz sine-wave generator, the carrier-modulation circuit, the PWM drive circuit, the ac power stage, and the ac output current detector sensor.

Frequency reference circuit: The frequency reference circuit provides a clock signal for all the timing systems in the inverter and converter modules, except in the low-voltage supplies. The operational amplifier in figure 31 is connected with a quartz crystal in the feedback loop operating at its natural resonant frequency. Resistors R2 and R3 provide dc paths for the input bias current of IC1, the oscillator. Resistor R1 controls the drive to the crystal. The R4-CR1-CR2 network converts the square-wave output of the operational amplifier into a logic level signal for IC2. For increased noise immunity, the remainder of the circuit was added, which produces a 20- to 24-volt peak-to-peak square wave for transmission within the modules and to other modules.

Countdown circuits: The frequency reference signal, a 20-volt peak-to-peak square wave, is converted back to a logic level signal by IC1 and the network on its input, as shown in figure 32. This logic signal is then divided to provide 9.6-kilohertz and 400-hertz signals and a 400-hertz repetition rate synchronizing signal. There are two basic styles of frequency dividers used in this circuit. The simplest is three stages of clocked binary (flip-flop) divide-by-two circuits. One stage is illustrated by IC18. The other technique is an all "NAND" gate divider. There are two of these circuits, one generates four 9.6-kilohertz, $90^{\circ}$-phase-shifted signals from the 38.4-kilohertz clock.

This is followed by the three binary counters, resulting in a 1.2-kilohertz signal, followed by the other NAND gate counter which produces three $120^{o}$-phase-shifted, 400-hertz waves. As shown in figure 32, the divide-by-four consists of gates IC2 to IC17. IC pairs 2-6, 3-7, 4-6, and 5-7 function as set-reset flip-flops with the inputs interconnected so that only one output can be low at any time. Gates, IC10 to IC13 are connected to determine the counting direction. Only one of the outputs of IC10 to IC13 is low at any time, so IC14 to IC17 are connected to add pairs of outputs together to produce square waves with $90^{o}$ relative phase shifts at the outputs A, B, C, and D.

To ensure correct phase displacement between different modules, a synchronizing line is provided to reset all the counters every 2.5 milliseconds. The synchronizing pulse is generated by "AND"ing together, with the clock signal, one of the 9.6-kilohertz outputs, the output of each binary counter, and one of the 400-hertz outputs. This produces a 26-microsecond wide synchronizing pulse every 2.5 milliseconds. This pulse is fed back into the counter and the counters of all the other inverter modules. Figure 33 shows the outputs of the countdown circuit.

400-Hertz sine-wave generator: The 400-hertz sine-wave reference is formed by passing a square wave through a pair of high-Q filters. Four of the outputs of the counter are three phase-shifted 400-hertz pulses with a $120^{o}$ dwell and a 1200-hertz square wave. IC1 and IC2 (fig. 34) combine these counter outputs to form a 400-hertz square wave at the output of IC2, as shown in figure 35. Only two 400-hertz counter outputs and the 1200-hertz output are used to generate the 400-hertz square wave. T1-C1 and T2-C3 are high-Q, L-C filters. IC3 is a buffer to prevent loading of the filter and to provide a low output impedance. Adjustment of R9 adjusts the output voltage to approximately 10 volts peak to peak.

The modulation gate is the diode bridge CR7-CR10 and the associated bias network. With a zero input, the bridge diodes are back biased by the current through R6 and only a small current flows through R7. The sine-wave output is very low. When the input is high (logic level 1), the diodes are forward biased and appear as a very low impedance. The sine-wave output is then approximately 10 volts peak to peak.

The three transistors and related parts are a phase correction network. Transistor Q3 senses the positive-going zero crossing of the sine-wave output and, by turning on Q1, effectively shunts R1 with R2 if the output of IC2 is positive. If the output of IC3 is precisely $180^{o}$ out of phase with the output of IC2, then the IC2 output is low while Q1 is turned on. Then the phase correction loop does nothing because diode CR1 blocks R2 from shunting R1. If the output of IC3 is delayed, then when the IC2 output goes positive, R2 will shunt R1 for the time of overlap, tending to shift the phase of the output forward. The same type of action occurs to retard the output phase. Figure 36 shows the square-wave output of IC2 and the sine-wave output of IC3.

Carrier-modulation circuit: The 9.6-kilohertz square-wave carrier signals are integrated to form triangular waves and are compared to the reference sine wave to form the PWM waveform.

Integrated circuit IC1 in figure 37 is IC14 (or IC15, IC16, or IC17) of figure 32. Its square-wave output is integrated by IC2. R1 and C2 determine the integrator time constant, with R1 adjusted to give a 10-volt peak-to-peak output. C1 provides dc isolation from IC1, since the output of IC1 is not symmetrical about the zero voltage axis. R2, R3, and C3 form a dc feedback path; C3 acting to reduce the ripple which is fed back.

The triangle wave is applied to one input of the operational amplifier comparator, (IC3) and the reference sine wave is applied to the other. This operational amplifier operates open loop and without frequency compensation for maximum switching speed. Figure 38 shows the two inputs and the output of the comparator. There are four of these circuits to generate the four-phase PWM signal.

PWM driver circuit: The four driver circuits, one for each phase of the carrier, are identical. Each is push-pull transformer coupled and supplies about 1 watt of peak drive power to each output transistor. The two gates shown in figure 39(a) increase the switching speed of the PWM wave and invert it (IC3). IC2 and IC4 are Darlington power transistors, shown schematically in figure 39(b). C1-R1 and C2-R3 are speedup networks to decrease the turnon and turnoff time. Diodes CR1 and CR3 prevent the power transistor from saturating by diverting drive current away from the base whenever the collector voltage falls more than 0.7 volt below the base emitter voltage. The drive transformer must be wideband to pass the 400-hertz fundamental and the switching waveform.

ac power stage: A simplified drawing of one-quarter of the output stage is shown in figure 40. It is a half-bridge, with transformer coupled push-pull drive and series "shoot-through" inductors L1 and L2 (ref. 8) to limit the collector currents during the switching interval when both transistors may be on simultaneously due to stored charge. The filter is low pass, but C1 is included to resonate with L3 at 400 hertz to obtain a low resistive output impedance. In the actual circuit (fig. 41), antisaturation drive circuits and reactive diodes are added. Whenever the collector voltage of Q2 plus the forward drop of CR1 is less than the base-emitter voltage of Q1 and Q2 plus the forward drops of CR2 and CR3, drive current through R1 for Q1 will be diverted through CR1 into the collector circuit of Q2. Transistor Q1 then reduces its collector current, limiting the drive to Q2 so that it will be just on the edge of saturation. This effectively eliminates the storage time of Q2 lessening the shoot-through problem. Also, the drive power is nearly proportional to the collector current, to improve the low-power efficiency. Diode CR4 reverse biases the base-emitter junction of Q2 during the off interval, and CR5 and CR6 limit the peak negative base voltage. The reactive diodes are CR8 and CR15, and are connected

before the shoot-through reactors L1 and L2 since they are included in the inductive part of the filter. Diodes CR7 and CR16 are normally nonfunctional, but serve to protect the transistors from reverse voltages. Diode CR17 is included to protect the polarized electrolytic capacitor C1 from reverse voltages.

The simplified schematic showing all four half-bridges is shown in figure 42. The two half-bridges on each side of the load have their carriers $180^{\circ}$ out of phase, and $90^{\circ}$ out of phase with the bridges on the other side. The 400-hertz fundamental is in phase on each side of the load, but $180^{\circ}$ out of phase with respect to the other side of the load. The output voltages of each bridge, referenced to -V, are shown in figure 43. The upper trace corresponds to the left-most bridge, the second trace to the second bridge from the left, etc.

The collector current of a power stage transistor for two cycles of 400-hertz output is shown in figure 44. The output of the inverter after filtering compared to the 400-hertz reference is shown in figure 45. The waves are in phase except for a slight ($\pm 2^{\circ}$) shift across the resonant output filter.

ac output current detector sensor: This circuit has two functions, the first of which is to provide a voltage proportional to load current. This is accomplished (fig. 46) with a current transformer (T1), its burden (R1), bridge rectifiers CR1 to CR4, and filter R2-C1. Q1 is an emitter follower to supply a low output impedance for noise consideration.

The second function is controlling the startup after a short circuit. In the event of a short circuit, this circuit is too slow; and a trip signal is sent out by a different circuit, shutting off the drive supply and recycling the startup circuit. The pulse also trips silicon controlled rectifier SCR1 in figure 46, charging C1 to nearly -12 volts. When C1 is completely charged, the current in SCR1 decreases and it commutates. As C1 slowly discharges, the inverter turns on into the short circuit with the regulator already in an overcurrent-limited mode, eliminating the transient condition of turning on suddenly into a short.

Converter system. - The converter system consists of the carrier generator and the pulse-width-modulator driver and power stages.

Carrier generator: The pulse repetition rate for the dc-to-dc converter PWM stage is generated in one of two ways. If the system is set up as a converter system only and there are no inverter modules, then IC1 to IC4 in figure 47 form a multivibrator. IC1 and IC3 are monostable multivibrators, and with the gates IC2 and IC4 for inversion, form a free-running square-wave oscillator. In normal operation (i.e., with an inverter module) but operating as either an inverter or converter, the inhibit jumper is connected, which blocks the free-running operation. A 9.6-kilohertz synchronous input repeatedly trips IC1, which puts out a pulse approximately one-half the width of a 9.6-kilohertz period. This synchronized operation avoids some noise problems. Integrated circuits IC3 and IC4 have no use in this mode of operation.

Two integrators are used to form the triangular waves which are the two carriers. These waves do not have to be extremely linear as in the ac stage, where a distorted carrier would result in a distorted output; so the integrators are simpler. C7 and C8 are used for noise consideration; resistors R5 and R6 maintain dc stability.

Pulse width modulator - driver stage: The modulator section in figure 48 is identical to the inverter system, except the reference signal is a dc control voltage instead of a sine wave. The operational amplifier is used to drive a single transistor directly as the driver is not a push-pull system and the power and speed requirements are much less severe.

The carrier is approximately 5 volts peak to peak, and the control voltage varies from about 3 volts at no on time, to slightly less than 0 volt for a conduction time slightly greater than 50 percent. The operation of the modulator is illustrated in figure 49.

Power stage: One of the two power output stages, including its current feedback drive circuit, is shown in figure 50. Current feedback is through T2, a 5:1 ratio transformer in the emitter of the output transistor Q2. This current passes through CR2 and Q1 to the base of Q2. There will also be a negative voltage developed on the third winding of T2, but it will not be sufficiently large to overcome the zener voltage of CR5. When the output of T1 (which is the output transformer of the driver stage) goes negative, Q1 is turned off. Since current can no longer flow through CR2 and Q1, the voltages on T2 rise. The increased voltage breaks down CR5, and a current flows out of the base of Q2, turning it off rapidly. This current will continue until Q2 stops conducting. C1 and CR3 prevent voltage spikes from breaking down Q1, and CR1 holds Q1 slightly out of saturation. In the actual circuit, Q1 is replaced by two Darlington-connected transistors, and there are several zener diodes used to suppress voltage spikes across the transformer.

Transformer T3 is an energy storage element. Whenever energy is being put into the primary, CR8 is back biased so no energy is being removed from the secondary. When Q2 turns off, the transformer voltage reverses and the energy stored in the magnetic field flows into the load through CR8. The various transformer waveforms are shown in figure 51. The rate of primary current rise is determined by the inductance of the primary winding, and the output voltage is determined by the load and the duty cycle. Figures 52 to 55 illustrate the waveforms at important parts of this circuit.

Control circuits. - The control circuits include the startup circuits, the voltage and current regulators, the dc sensors, and the low-voltage power supplies.

Startup circuits: The startup circuit for the inverter and converter submodules determines the output voltage and controls the 20-volt supply, modulation gate, and converter control voltage. This circuit programs two different startup modes, depending on the output voltage. In general, the output voltage is zero if the inverter is off; and IC1 (fig. 56) puts out a low signal, turning on the 20-volt drive supply but holding the modula-

tion gate and control voltage off. After a time delay of 0.2 second caused by IC7, the modulation gate turns on. This also turns Q1 off, allowing C3 to discharge through R12. As C3 discharges, the converter control voltage and the output voltage slowly ramp on. A startup is shown in figure 57.

As the output voltage rises, IC1 turns off; but a path through IC5, IC6, IC8, and IC4 has formed a latch so that nothing happens. At approximately 70 percent output, IC2 turns on. This unlatches the IC5-IC6-IC8-IC4 circuit, but holds the inverter on through a path through IC5, IC3, IC10, and IC11. If the output drops below 70 percent, however, IC2 turns off; the 20-volt supply opens; the modulation gate, controlled by IC10, opens; and Q1 and Q2 clamp the control voltage off. The output voltage then normally falls to zero, and the circuit restarts. If the inverter is in parallel with another unit, an inverter could turn off, but the output could still be normal (120 V). Then IC2 turns on, followed immediately by the modulation gate with no time delay. The control voltage still ramps on.

The voltage trip points are set by the voltage dividers R1-R2 and R6-R7 at the operational amplifier inputs and the reference formed by CR3. CR2 and CR4 clamp the operational amplifier output to logic level voltages. C2 and R10 determine the monostable multivibrator time delay for the modulation gate. This circuit is contained in the converter submodule but controls both the inverter and the converter.

Voltage and current regulators: Voltage and current regulation is accomplished by varying the control voltage to the dc-to-dc converter modulator. Four circuits are OR'd together, such that the highest voltage has control, and the highest voltage corresponds to the shortest duty cycle and lowest output power in the converter. This is accomplished by CR2, CR3, CR10, and CR11 in figure 58. Each of the four regulators of figure 58 uses an operational amplifier with closed-loop feedback; and they are all always connected, even though in the converter mode the ac voltage and current regulators do nothing. The gain of the two voltage regulators containing IC1 and IC2 is determined by a nonlinear feedback loop to compensate for the very nonlinear control voltage - output power plot of the converter. A plot of the regulator characteristics is shown in figure 59. For IC1 (fig. 58) as the control voltage rises above 0.5 volt, CR1 and Q1 begin to conduct, effectively removing R4 and R5 from the feedback loop. Since R3 is much larger than R4 and R5, the gain increases significantly for large output (control) voltages. There is a similar loop for IC2, although the use of two diodes raises the break point to approximately 1.5 volts.

The ac regulator senses the average voltage from the feedback transformer T1. Resistors R15 and R16 are dependent controls which adjust the output voltage and gain interdependently. Both overcurrent regulators compare the output of their respective current-to-voltage transducer to a reference voltage set by R23. When the transducer voltage exceeds this set point, the operational amplifier output swings positive and limits

the output power by controlling the modulation index of the converter in a somewhat linear manner. The dc overcurrent regulator, because of the transducer design, also regulates to a converter overvoltage point. An overvoltage transient often occurs during load switching or startup due to the slow response of the output voltage regulators.

R32 is connected to a voltage proportional to the input voltage. It raises the control voltage slightly at high input voltage to reduce the tendency of the converter to increase its output at higher input. This input voltage compensation makes the inverter output voltage almost independent of input voltage.

dc sensors: The input for the two dc voltage and current regulators and the ac short-circuit trip are obtained from three chopper-rectifier circuits (fig. 60). These circuits sense either dc link voltage or current by means of shunts. The choppers are driven by the 2-kilohertz oscillator in the power supply. The uppermost chopper measures link voltage through R5, CR1 or CR2, and CR3. It also measures current through R3. This current actually corresponds to the peak collector current in the output stage transistors of the converter.

The second chopper senses the voltage across R12. In the event of a short on the inverter, excessive current will be drawn through this resistor as the converter output filter capacitor C2 discharges. The output of this sensor is used to trip off the 20-volt drive supply.

The third chopper is used for 150-volt converter dc voltage regulation only. Resistors R22, R23, and R24 in conjunction with CR10 and Q9 form a voltage divider, which produces about 2 volts at the chopper primary for 150-volt dc converter output. Transistor Q9 creates a low impedance but also a relatively low power consumption divider.

Low-voltage power supplies: The low-voltage supply for the inverter converter system consists of a single multiple-output converter, three series-pass linear regulators, and a switching regulator with a "crowbar" and rather elaborate controls.

The converter is shown in figure 61. It is powered directly from the unregulated input voltage, and supplies about 50 watts of output power. It also powers the chopper transformers in figure 60 by means of auxiliary windings. Transformer T1 sets the operating frequency, which is approximately 2 kilohertz and proportional to the input voltage. CR2 to CR7 and R5 limit the peak collector current during switching by diverting the base drive if the base emitter voltage of the transistor plus the voltage across R5 is greater than the total forward voltage of the diodes.

The 20-volt switching regulator is shown in figure 62. It uses a Schmitt trigger, Q1 and Q2, to drive a quasi-Darlington pair, Q3 and Q4. CR3 and CR4 shut off the regulator when the trip signal is a logical 0, ground.

The crowbar and controls for the 20-volt regulator are shown in figure 63. There are five inputs to this circuit, any one of which will turn off the supply. One input is the trip signal from the startup circuit, which has been discussed. The second is a time delay driven from the 6-volt supply to ensure the countdown circuits and regulators have

stabilized before drive is applied. This circuit involves Q1, IC1 (a schmitt trigger), and the related parts. The third signal is a pulse which indicates that the contactor supplying input voltage to the inverter machine is going to open, and assures smooth turnoff. The fourth trip is the shutoff caused by a short circuit on the inverter. These inputs are all AND'd by IC6. The fifth trip involves Q3, etc. It holds off the supply until the 6-volt supply has come on, so that the delay involving IC1 will operate.

Any trip pulse clamps the output of IC7 to ground, turning off Q4. This supplies a drive to silicon controlled rectifier SCR1 through R11 and CR8. SCR1 turns on, crowbarring the 20-volt supply and turning on Q5, which supplies the trip signal for the 20-volt switching regulator (fig. 62). This supply automatically recycles, because the holdoff signal turns off the regulator; so SCR1 commutates, which releases the holdoff and the regulator restarts. R8, R9, and Q2 supply a signal to the ac overcurrent detector (fig. 46) in case of a short-circuit trip.

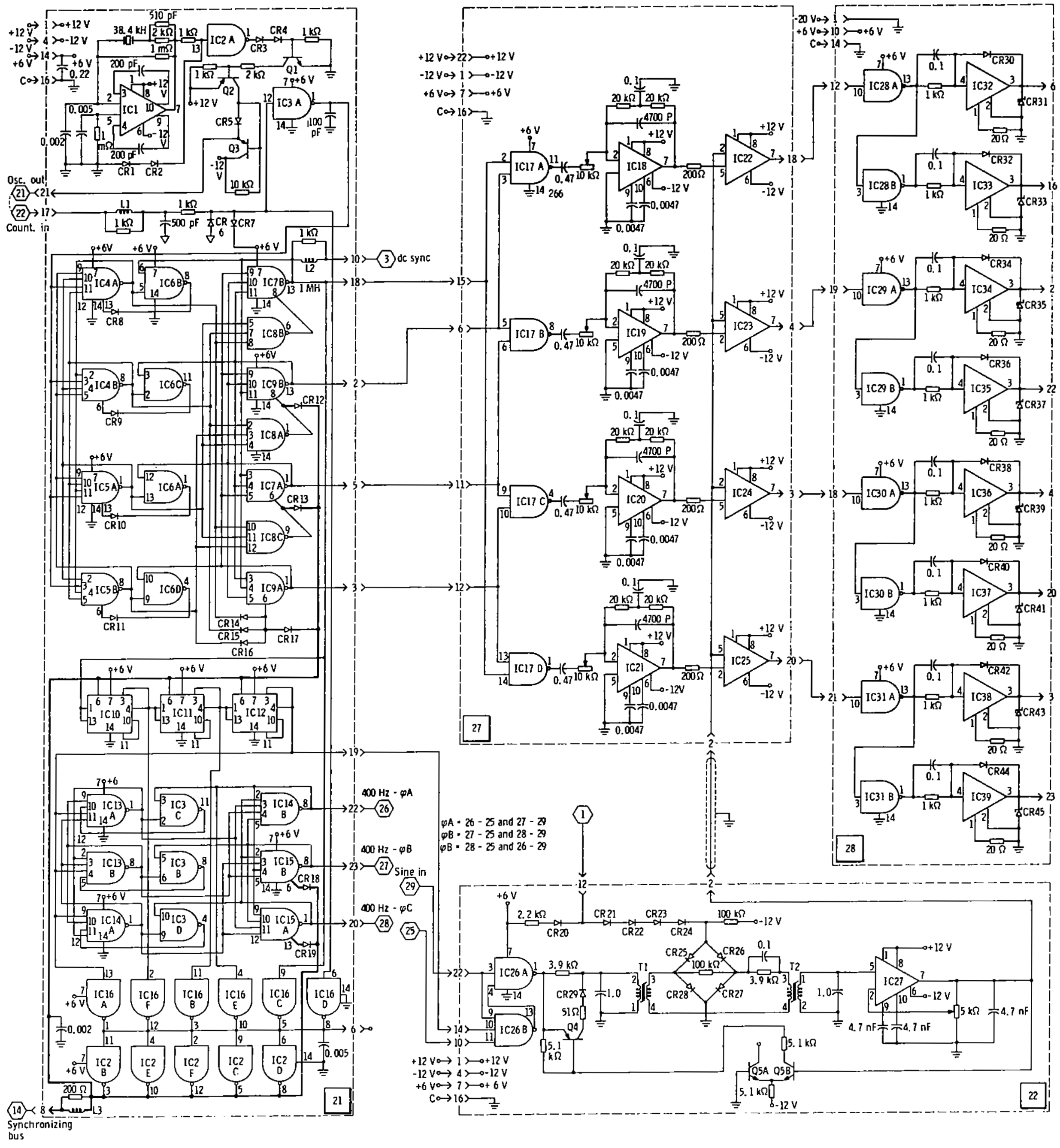
The complete circuit, with component valves, is presented in appendix C.

# APPENDIX C

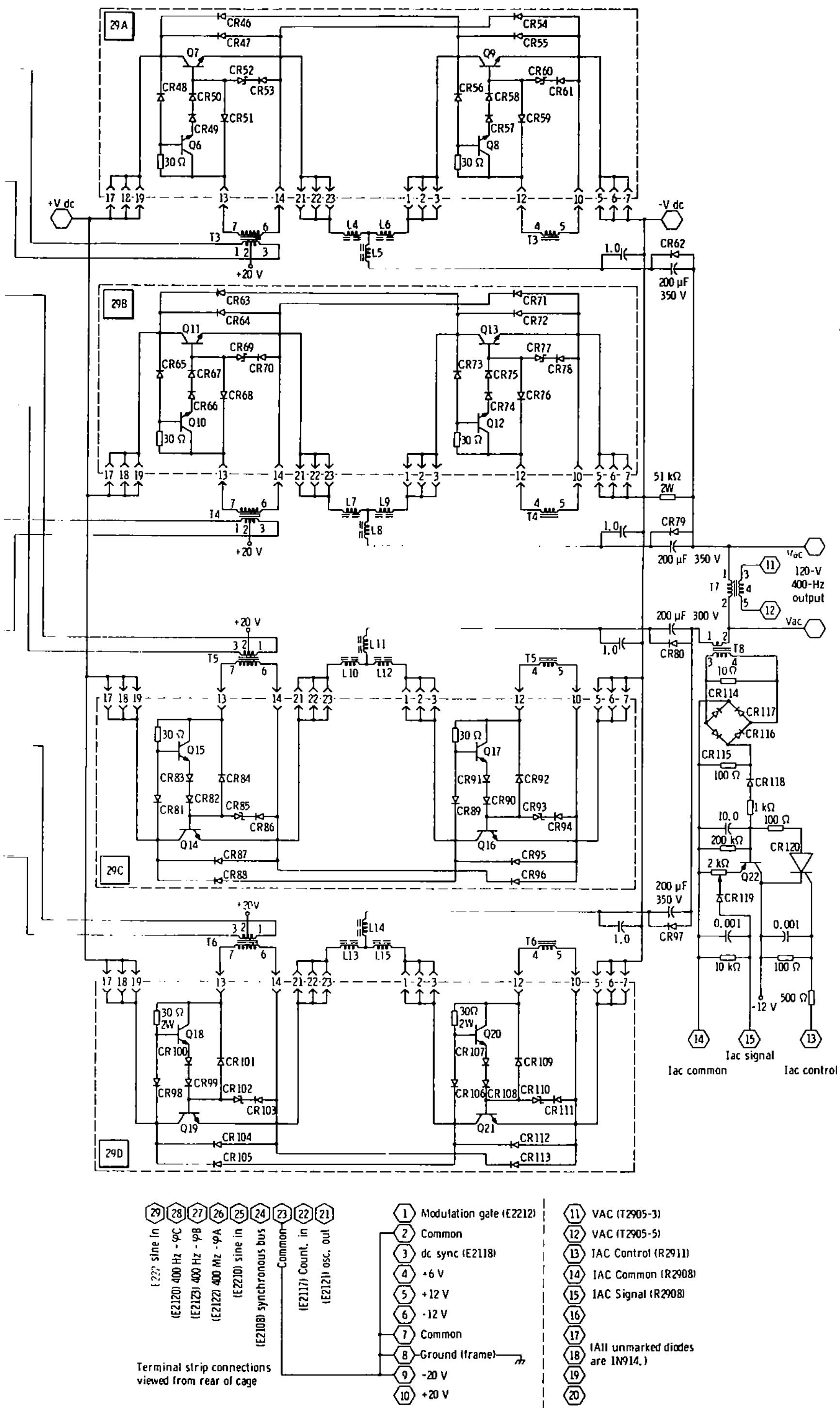
## COMPLETE PART LISTS AND SCHEMATICS FOR INVERTER AND CONVERTER SUBMODULES

### Inverter Submodule

| | |
|---|---|
| CR1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 114, 115, 116, 117, 118, 119 | 1N 914 |
| CR30, 32, 34, 36, 38, 40, 42, 44 | UTR 12 |
| CR31, 33, 35, 37, 39, 41, 43, 45 | 1N 3039 |
| CR46, 54, 63, 71, 88, 96, 105, 113 | 1N 3893 |
| CR47, 55, 64, 72, 87, 95, 104, 112 | 1N 1204A |
| CR48, 56, 65, 73, 81, 89, 98, 106 | UTR 62 |
| CR49, 50, 51, 57, 58, 59, 66, 67, 68, 74, 75, 76, 82, 83, 84, 90, 91, 92, 99, 100, 101, 107, 108, 109 | UT 4005 |
| CR52, 60, 69, 77, 85, 93, 102, 110 | 1N 3826A |
| CR53, 61, 70, 78, 80, 94, 103, 111 | UT 261 |
| CR62, 79, 80, 97 | UT 4040 |
| CR120 | 2N 2413 |
| Q1 | 2N 2219A |
| Q2, 3 | 2N 2907 |
| Q4, 22 | 2N 2905A |
| Q5 | 2N 2916 |
| Q6, 8, 10, 12, 15, 17, 18, 20 | 2N 2697 |
| Q7, 9, 11, 13, 14, 15, 19, 21 | SDT 8664 |
| L1, 2 | 1 mH |
| L3 | 170 μH |
| L4, 6, 7, 9, 10, 12, 13, 15 | 50 μH, 21 A |
| L5, 8, 11, 14 | 1.0 mH, 21 A |
| T1, 2 (Resonant filter transformer) | 9:1 ratio |
| T3, 4, 5, 6 (Drive transformer) | 4:1 ratio |
| T7 (Output voltage feedback transformer) | 1:1 ratio |
| T8 (Current sense transformer) | 53:1 ratio |
| IC1, 18, 19, 20, 21, 22, 23, 24, 25, 27 | WS 161Q |
| IC2, 16 | WM 295G |
| IC3, 6, 17 | WM 266G |
| IC4, 5, 13, 14, 15 | WM 261G |
| IC7, 9, 26, 28, 29, 30, 31 | WM 220G |
| IC8 | WM 227G |
| IC10, 11, 12 | WM 215G |
| IC32, 33, 34, 35, 36, 37, 38, 39 | WS 145 |



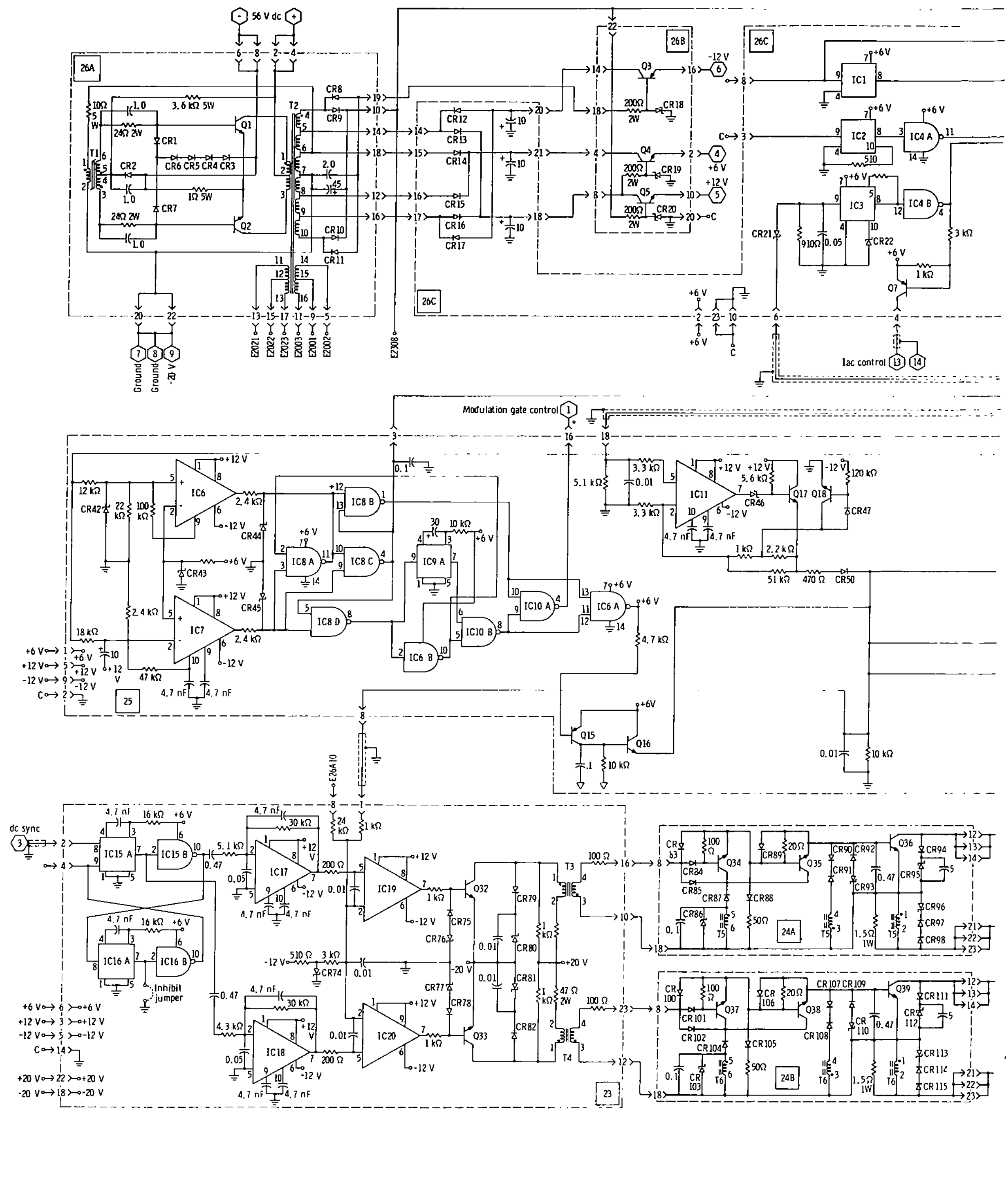
Schematic diagram



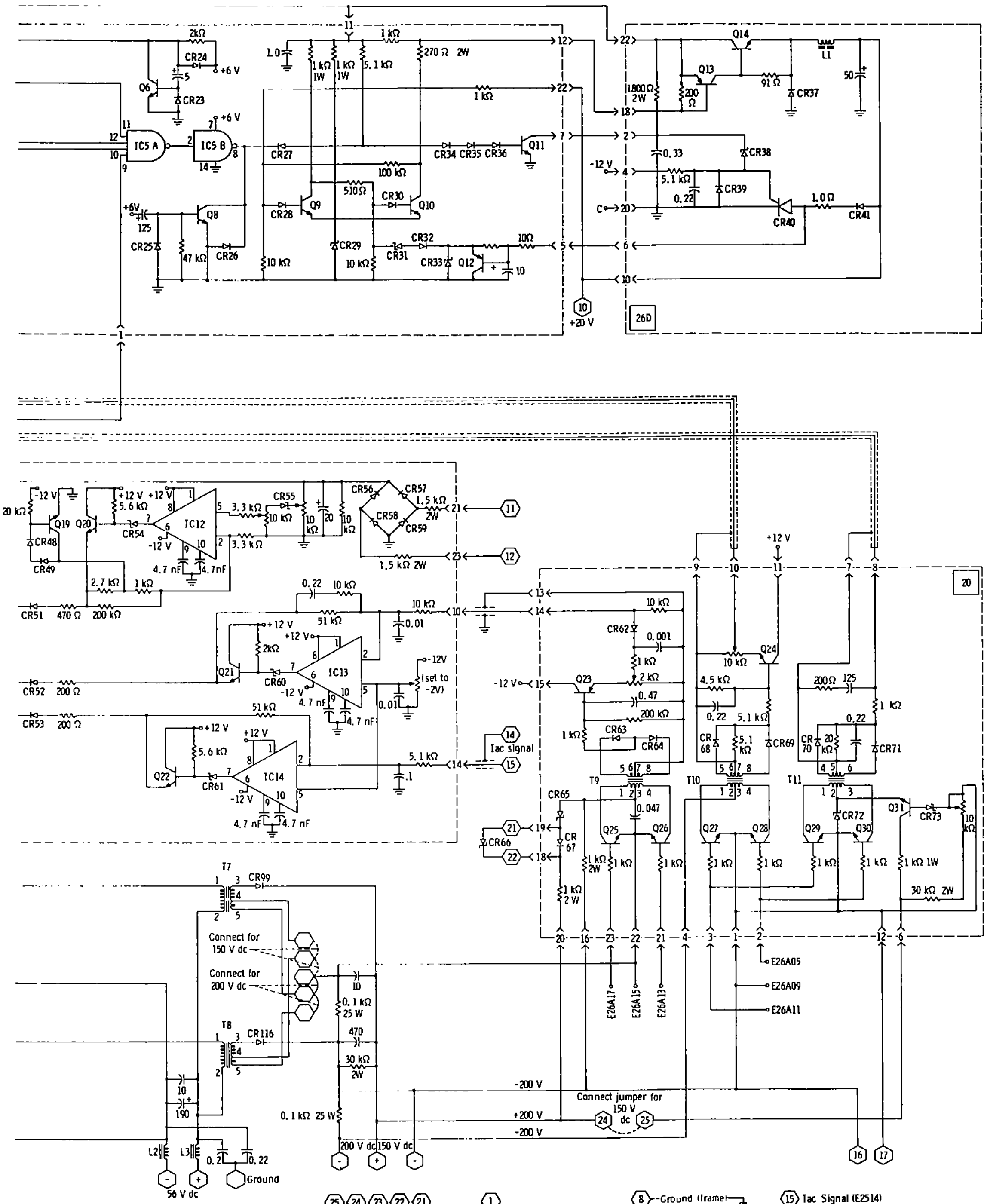

dc-to-ac inverter

| | |
|---|---|
| CR1, 3, 4, 5, 6, 7, 56, 57, 58, 59 | IN 649 |
| CR2 | UTR 2005 |
| CR8, 11, 14, 15, 41 | UT 4005 |
| CR9, 10 | 1N 1201A |
| CR12, 13, 16, 17, 94, 111 | UTR 62 |
| CR18 | 1N 2976RB |
| CR19, 38 | 1N 2970B |
| CR20 | 1N 2976B |
| CR21 | 1N 3821 |
| CR22, 43, 96, 113 | 1N 3824B |
| CR23, 24, 25, 27, 28, 30, 32, 34, 35, 36, 39, 47, 48, 49, 50, 51, 52, 53, 62, 63, 64, 68, 69, 70, 71, 75, 78, 79, 82, 83, 84, 85, 88, 89, 100, 101, 102, 105, 106 | 1N 914 |
| CR26 | 1N 3018B |
| CR29, 53, 73 | 1N 3027B |
| CR31 | 1N 3022B |
| CR33 | 1N 3028B |
| CR37, 87, 104 | 1N 3893 |
| CR40 | 2N 1772 |
| CR42, 44, 45, 74 | 1N 3016B |
| CR46, 54, 60, 61 | 1N 746 |
| CR65 | 1N 3012RB |
| CR66 | 1N 3020B |
| CR67 | 1N 3000B |
| CR72, 76, 77, 93, 110 | 1N 3828B |
| CR80, 81 | 1N 3039B |
| CR86, 103 | 1N 3033B |
| CR90, 92, 107, 109 | UTR 12 |
| CR91, 108 | 1N 3995 |
| CR95, 112 | 1N 3011B |
| CR97, 98, 114, 115 | 1N 5397 |
| CR99, 116 | ED 8312 |

| | |
|---|---|
| Q1, 2 | 2N 2580 |
| Q3, 13 | 2N 2023 |
| Q4, 5 | 2N 1016 |
| Q6 | MPS 6515 |
| Q7, 23 | 2N 2905A |
| Q8, 32, 33 | 2N 2405 |
| Q9, 10, 11, 17, 18, 19, 20, 21, 22, 24, 25, 26, 27, 28, 29, 30 | 2N 2222A |
| Q12 | 2N 3244 |
| Q14 | 2N 2811 |
| Q15 | 2N 722 |
| Q16 | 2N 718 |
| Q31 | DTS 411 |
| Q34, 37 | 2N 5262 |
| Q35, 38 | 2N 3714 |
| Q36, 39 | 34 AM 109/SDT 8653 |
| IC1, 2, 3 | WM 208G |
| IC4, 8, 10 | WM 266G |
| IC5 | WM 261G |
| IC6, 7, 11, 12, 13, 14, 17, 18, 19, 20 | WM 161Q |
| IC9, 15, 16 | WS 841Q |
| T1 (Timing transformer) | 2:1:1 ratio |
| T2 (Low-voltage converter output transformer) | 56-V input at 2 kHz; 28-V, 18-V, 10-V CT output; two chopper drive windings, 20V/ 10 kHz |
| T3, 4 (Drive transformer) | 1:1 ratio |
| T5, 6 (Current feedback transformer) | Pins 5-6, 20 turns; pins 3-4, 8 turns; pins 1-2, 4 turns |
| T7, 8 (Converter output transformer) | 1:3 or 1:4 ratio; primary inductance, 250 $\mu$H |
| T11 (Chopper transformers) | 1:1 ratio |
| T9, 10 (Chopper transformers) | 1:10 ratio |
| L1 (20-V regulator filter) | 200 $\mu$H; 6 A |
| L2, 3 (Input filter) | 50 $\mu$H; 30 A |



Schematic diagram



25 24 23 22 21

E2006 E2020 — dc jumper

E2018 E2019 — dc zener

1
2 Common
3 dc sync (E2302)
4 +6 V
5 +12 V
6 -12 V
7 Common (E26A20-22)

8 -Ground (frame)
9 -20 V
10 +20 V
11 Vac (E2521)
12 Vac (E2523)
13 Iac Control (E26004)
14 Iac Common (E2502)

15 Iac Signal (E2514)
16 dc load sharing (E2001)
17 dc load sharing (E2012)

(All unmarked diodes are 1N914.
All resistors 1/2 W unless marked.)

f dc-to-dc converter

# REFERENCES


1. Klimo, R. G.; Krejny, E. L.; Larson, A. B.; Resch, R. J.; and Murray, J. E.: Optimization Study of High Power Static Inverters and Converters. Rep. ER-6586, TRW, Inc. (NASA CR-54186), Sept. 14, 1964.

2. Peterson, W. V.; and Resch, R. J.: 5 KW Pulse Width Modulated Static Inverter. Rep. ER-6809, TRW Equipment Labs. (NASA CR-54872), Dec. 1, 1965.

3. Knight, Milton; and Torkildsen, Robert: 1 KVA Three-Phase DC-AC Inverter with Digital Control. Proceedings of the Fourth Intersociety Energy Conversion Engineering Conference. AIChE, 1969, pp. 854-860.

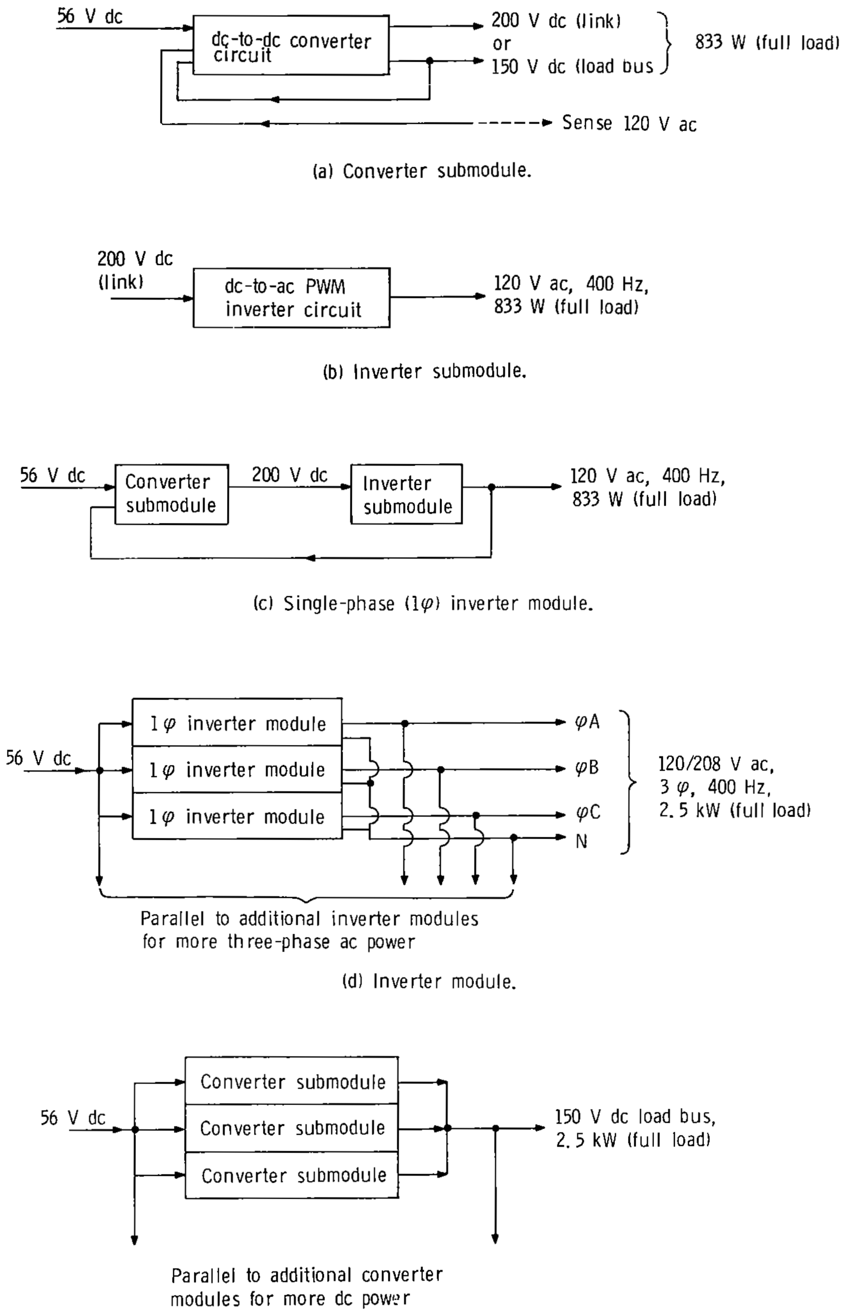
4. Gourash, Francis; and Birchenough, Arthur G.: Design Analysis and Performance of a 2.5 KVA Pulse-Width-Modulated Static Inverter. NASA TN D-5586, 1970.

5. Ravas, R. J.; Pittman, P. F.; and Briggs, R. W.: Staggered Phase Carrier Cancellation - A New Circuit Concept to Provide Lightweight Static Inverters. IEEE Trans. on Aerospace and Electronic Systems, Supplement, vol. AES-3, Nov. 1967, pp. 432-444.

6. Baker, Dwight: Single-Ended Switching Transformer Regulator. Research Achievements Reviews. Volume 1: Series 1 through 22. NASA TM X-53620, 1967.

7. Gourash, Francis; Pittman, P. F.; and Heins, J. F.: Modularization of High-Power Inverters and Converters. Proceedings of the Fourth Intersociety Energy Conversion Engineering Conference. AIChE, 1969, pp. 830-838.

8. Gourash, Francis: Analysis and Design of Inductors for Protecting Power Transistors Against Current Surges in Inverter Bridge Circuits. NASA TN D-4995, 1969.




(a) Converter submodule.

(b) Inverter submodule.

(c) Single-phase (1φ) inverter module.

(d) Inverter module.

(e) Converter module.

Figure 1. - Module nomenclature and modular systems concept.

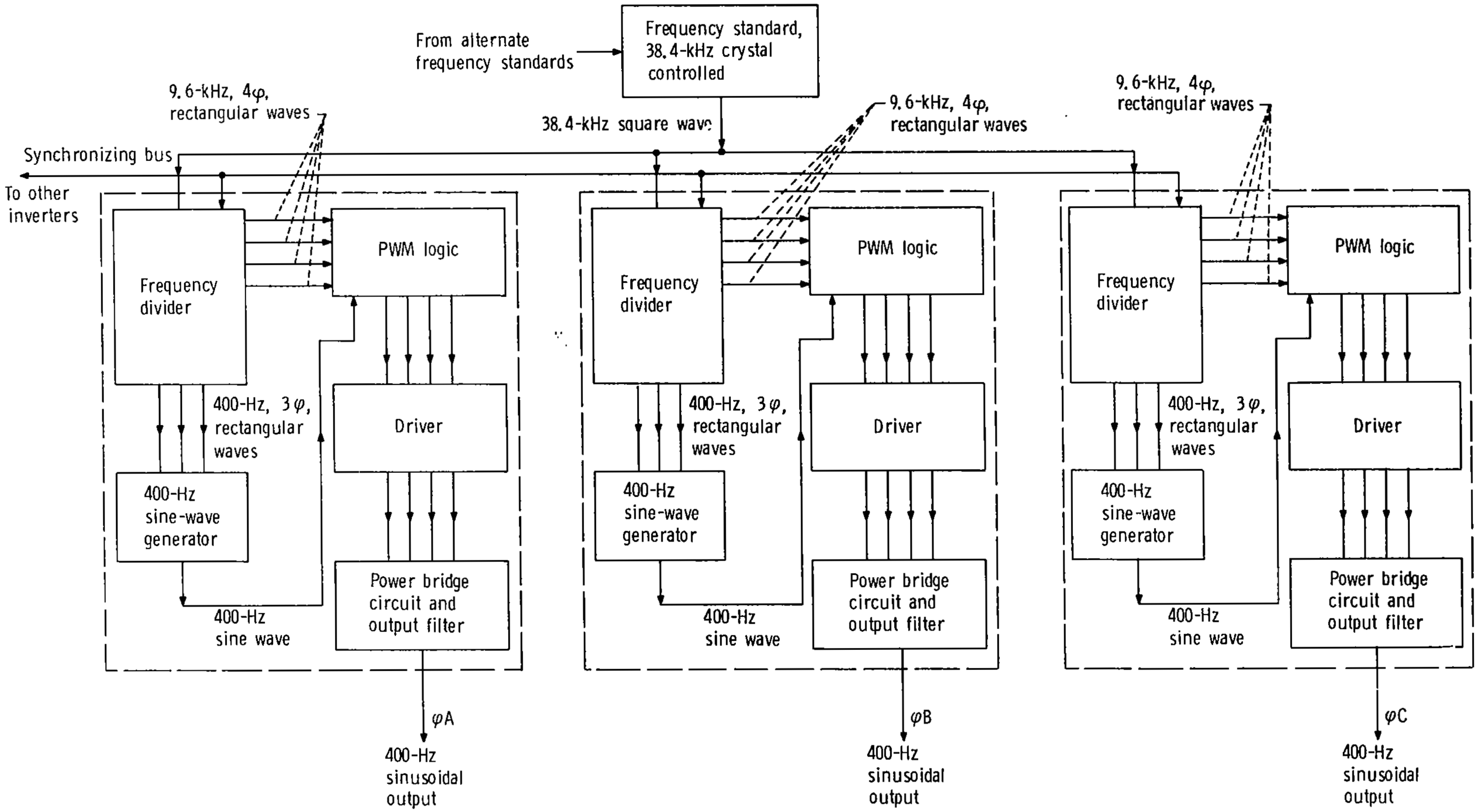



Figure 2. - Block diagram of inverter submodules interconnected for three-phase, 400-hertz output.

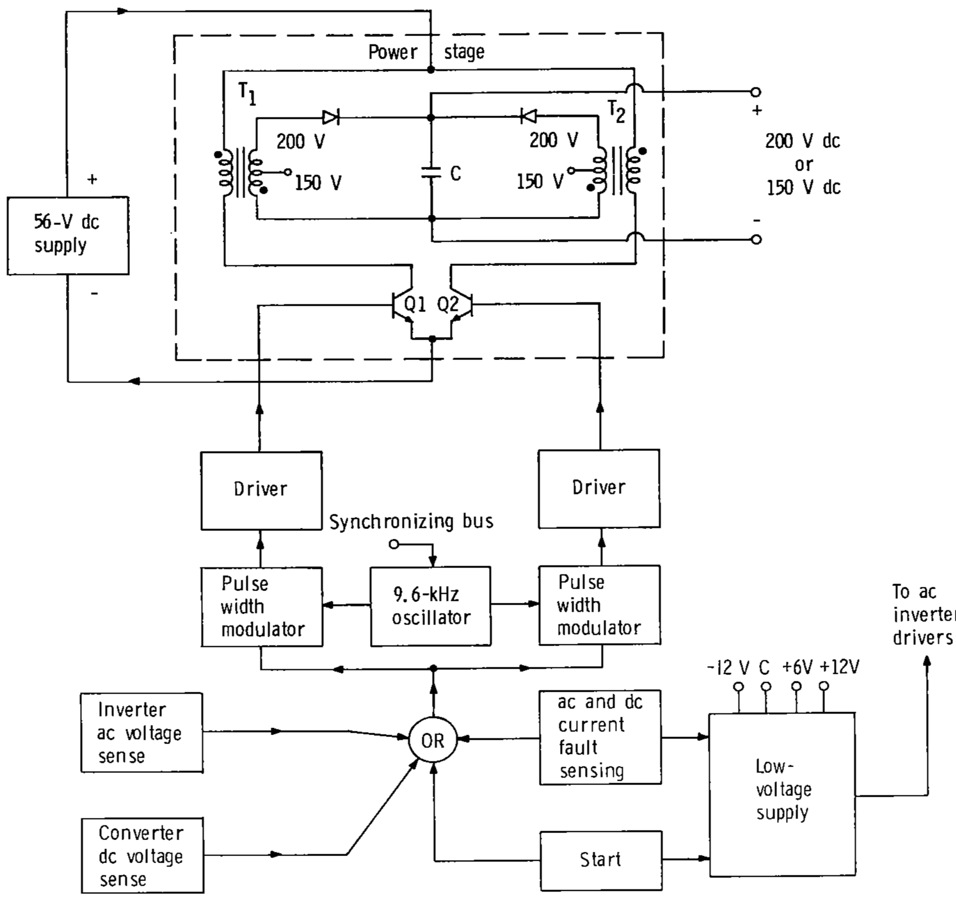



Figure 3. - Block diagram of dc-to-dc converter submodule.

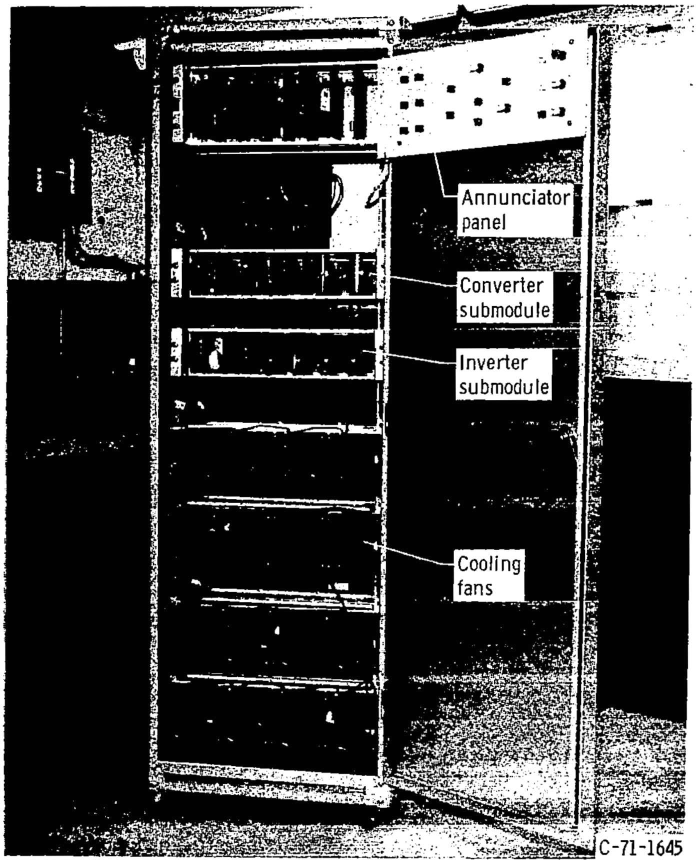



Figure 4. - Inverter module.

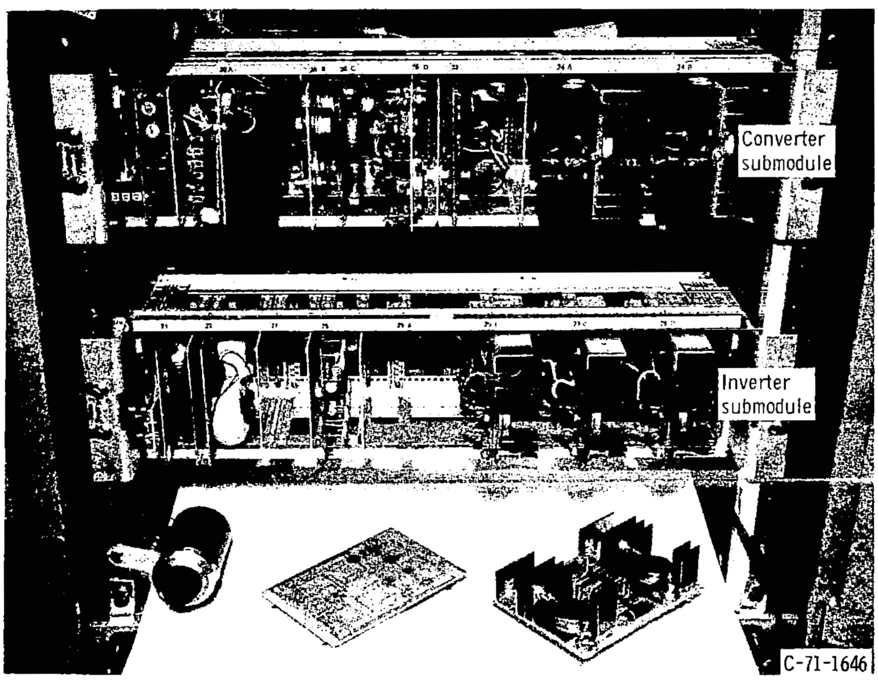



Figure 5. - Closeup views of converter and inverter submodules.

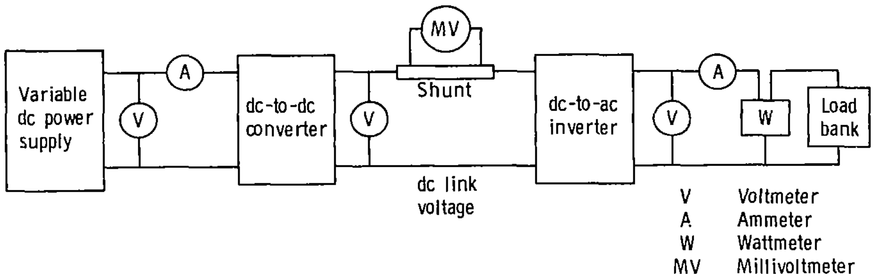



Figure 6. - Bench test circuit for single-phase tests.

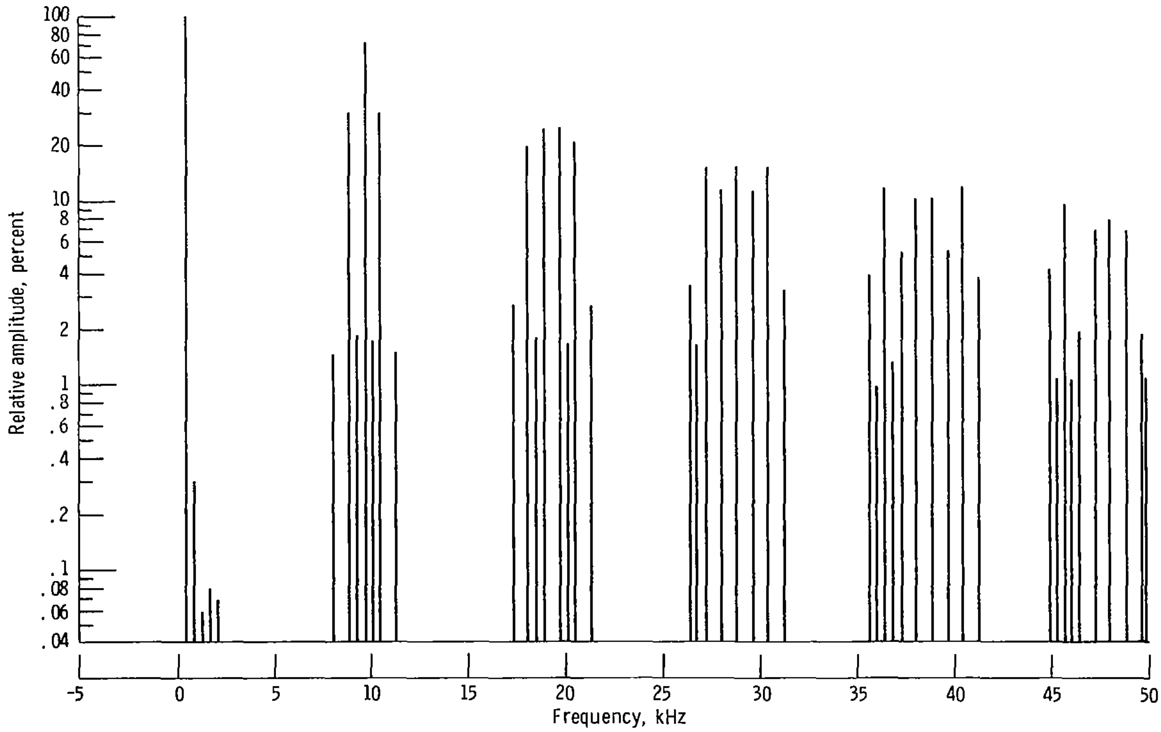



Figure 7. - Harmonic content of 9.6-kilohertz-carrier pulse-width-modulated signal - double-sided modulation. Total harmonic distortion, 104.7 percent; modulation index, 95 percent.

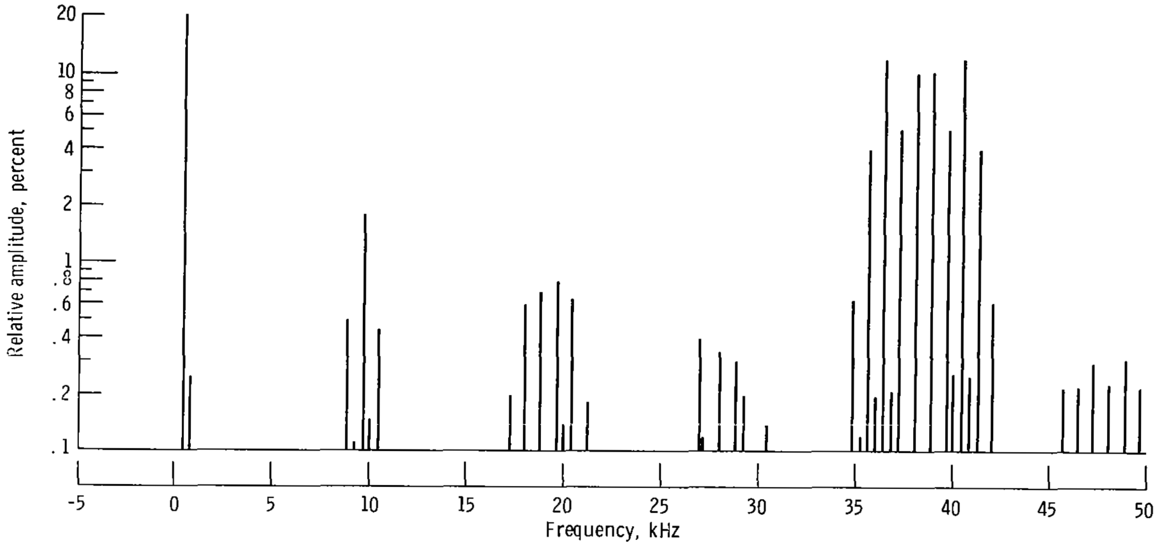



Figure 8. - Harmonic content of carrier-cancelled pulse-width-modulated voltage at input to ac output filters. Total harmonic distortion, 24.2 percent; modulation index, 95 percent.

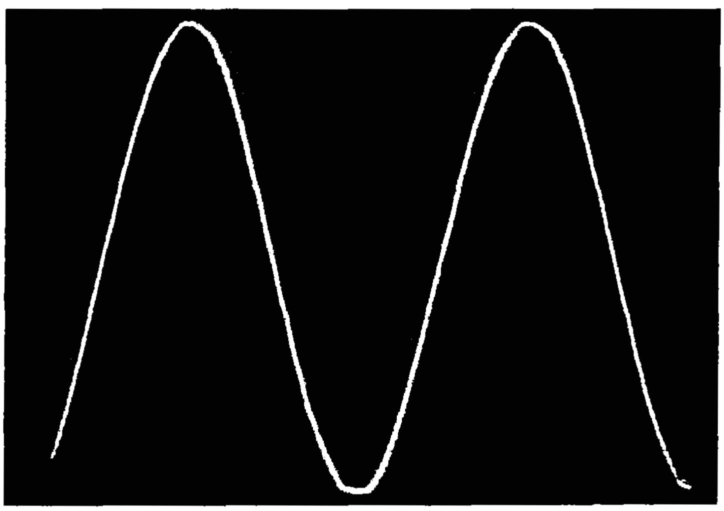


Figure 9. - ac output voltage. Vertical scale, 50 volts per division; horizontal scale, 0.5 millisecond per division.

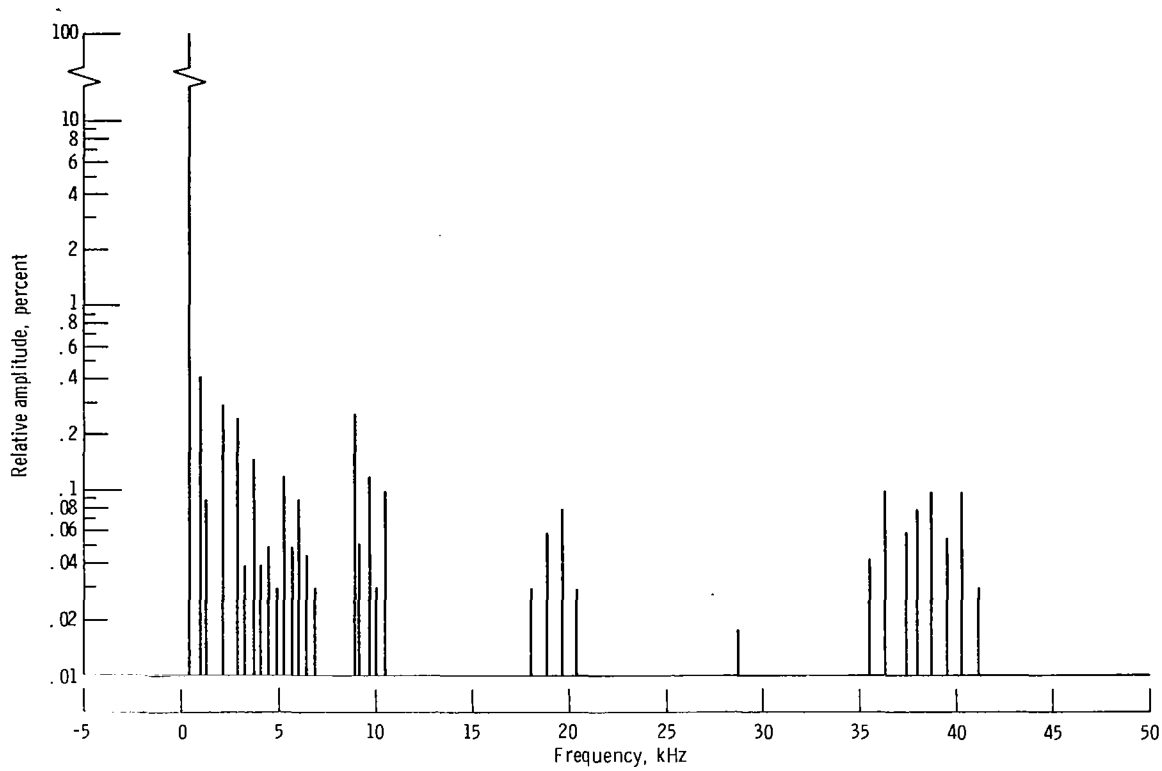
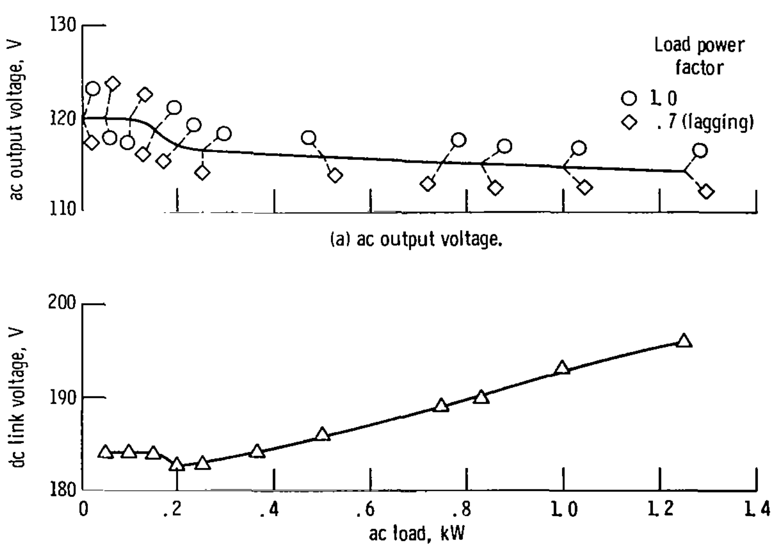



Figure 10. - Harmonic content of 400-hertz ac output voltage. Total harmonic distortion, 0.74 percent; modulation index, 95 percent.




(b) Converter submodule dc link voltage to inverter for ac load power factor of 0.7.

Figure 11. - Single-phase inverter module voltage regulation.

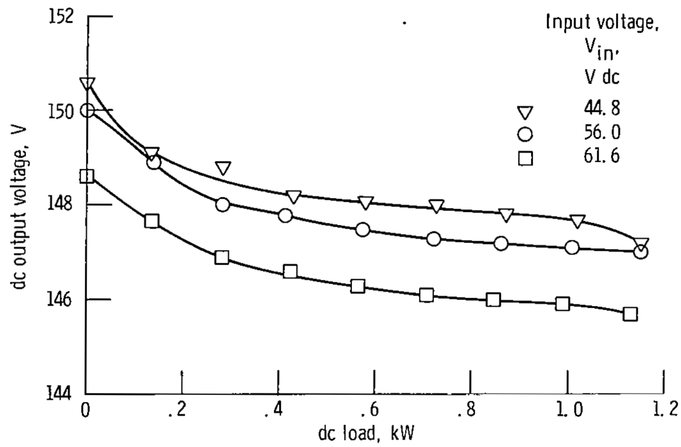



Figure 12. - Converter submodule voltage regulation.

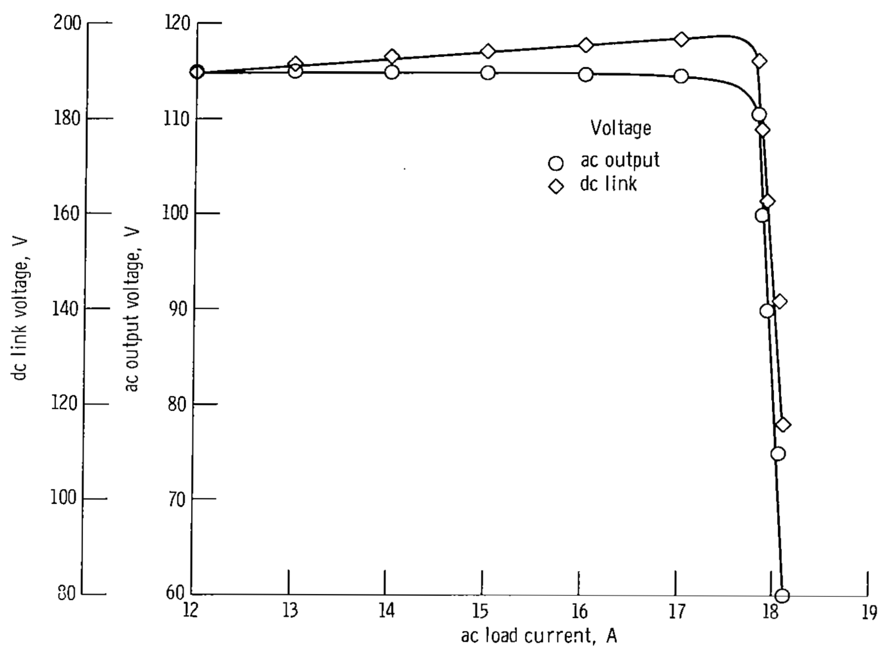



Figure 13. - Regulation of ac output voltage and dc link voltage in current-limit operating region.

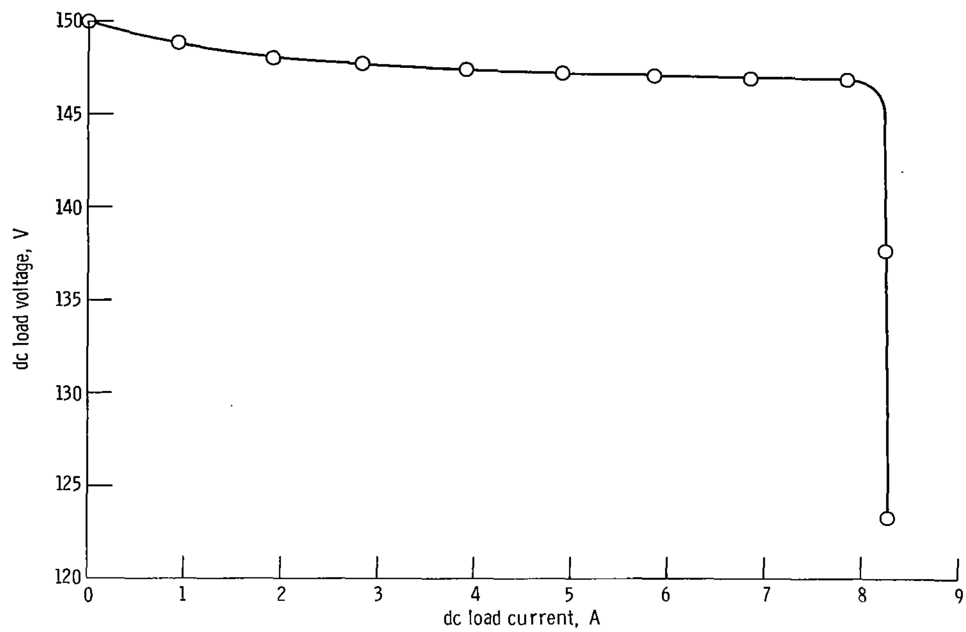



Figure 14. - Voltage regulation of converter submodule as function of load current extending into current-limit region. dc input voltage, 56.0 volts.

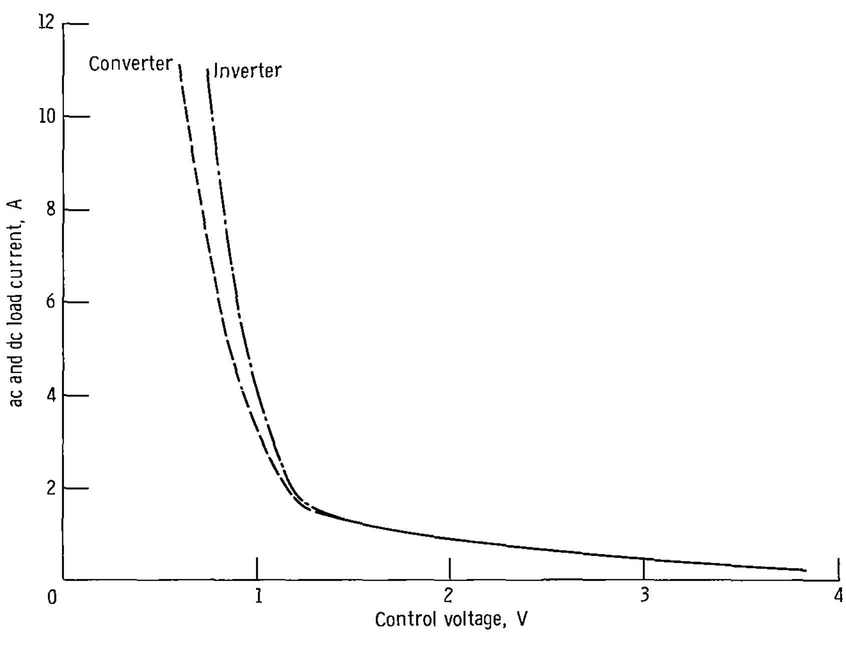



Figure 15. - Control voltage required for inverter and converter submodules for rated output voltage as function of load current. Rated output voltage: inverter, 120 volts (L-N); converter, 150 volts dc.

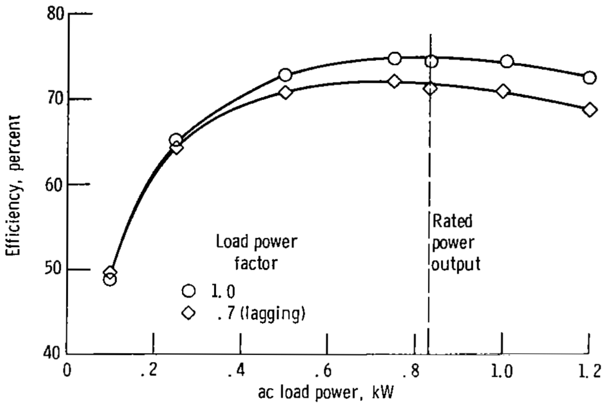



Figure 17. - Overall efficiency of single-phase inverter module for 0.7- and unity-power-factor loads and dc input voltage of 56 volts.

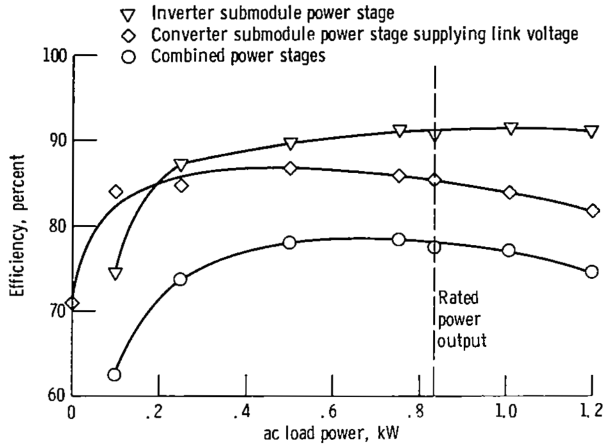



Figure 16. - Efficiency of single-phase-inverter-module individual power stages and combined power stages for unity-power-factor load and with dc input voltage of 56 volts.

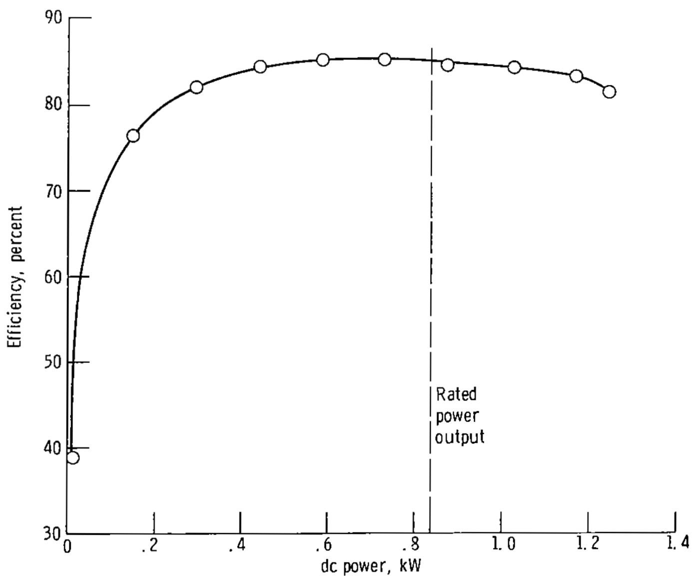



Figure 18. - Efficiency of converter submodule supplying 150 volts dc to a dc load. Input voltage, 56 volts dc.

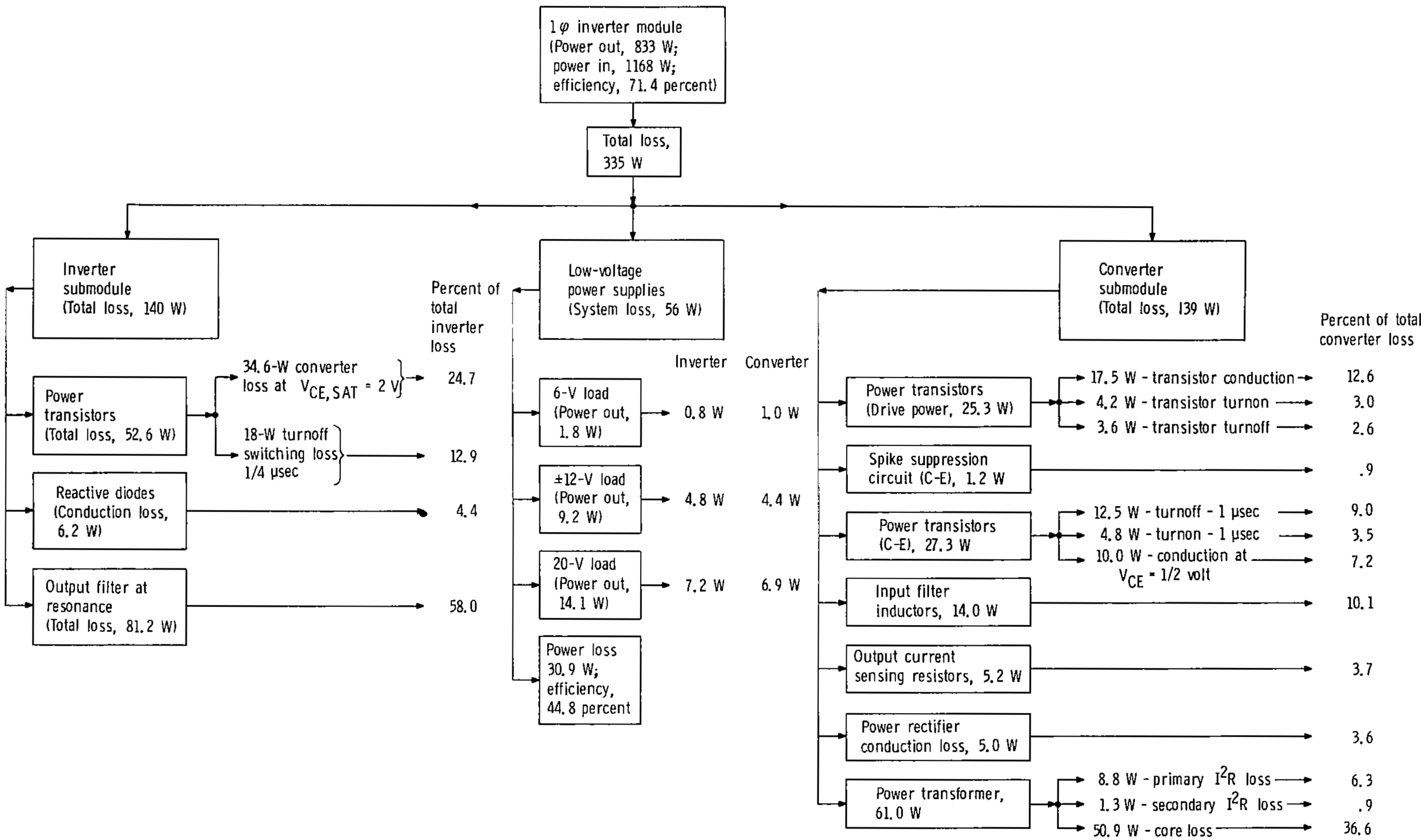



Figure 19. - Single-phase inverter module loss breakdown.

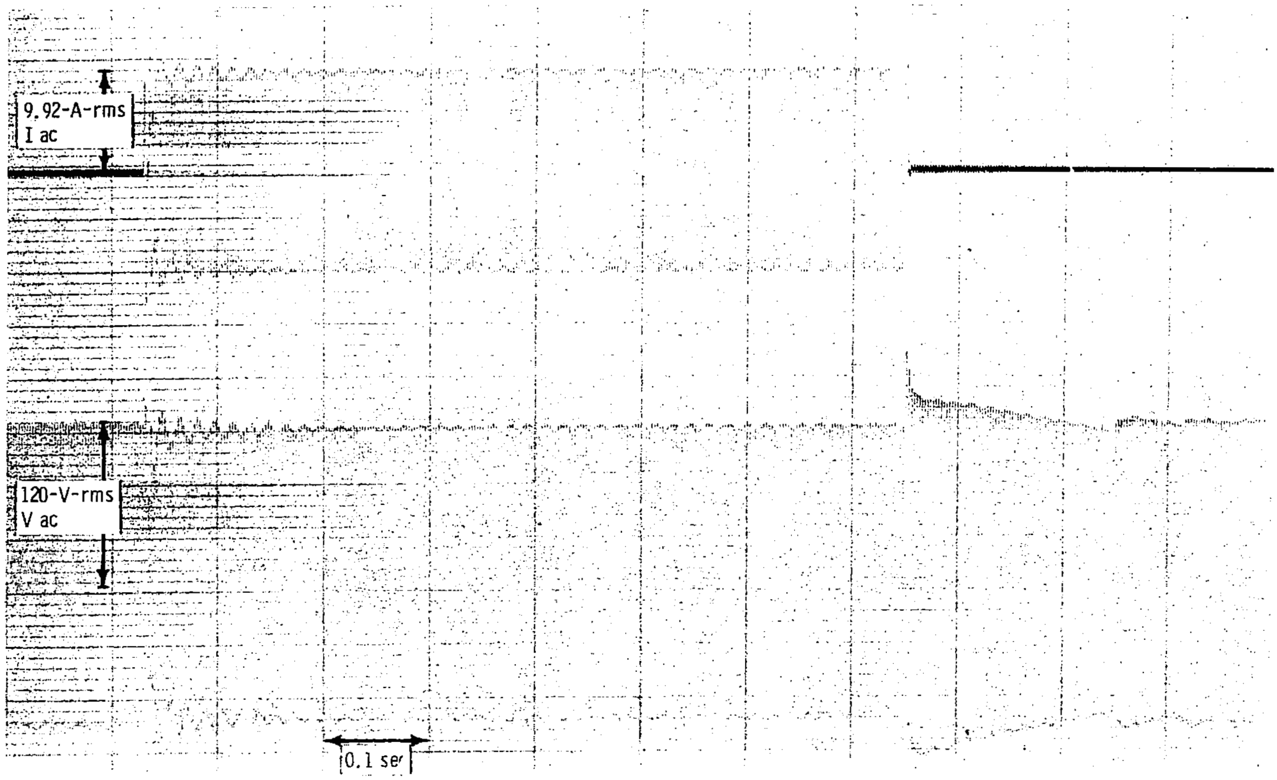



Figure 20. - Transient response trace of single-phase inverter module for step load change from zero to full rated load at 0.7 power factor.

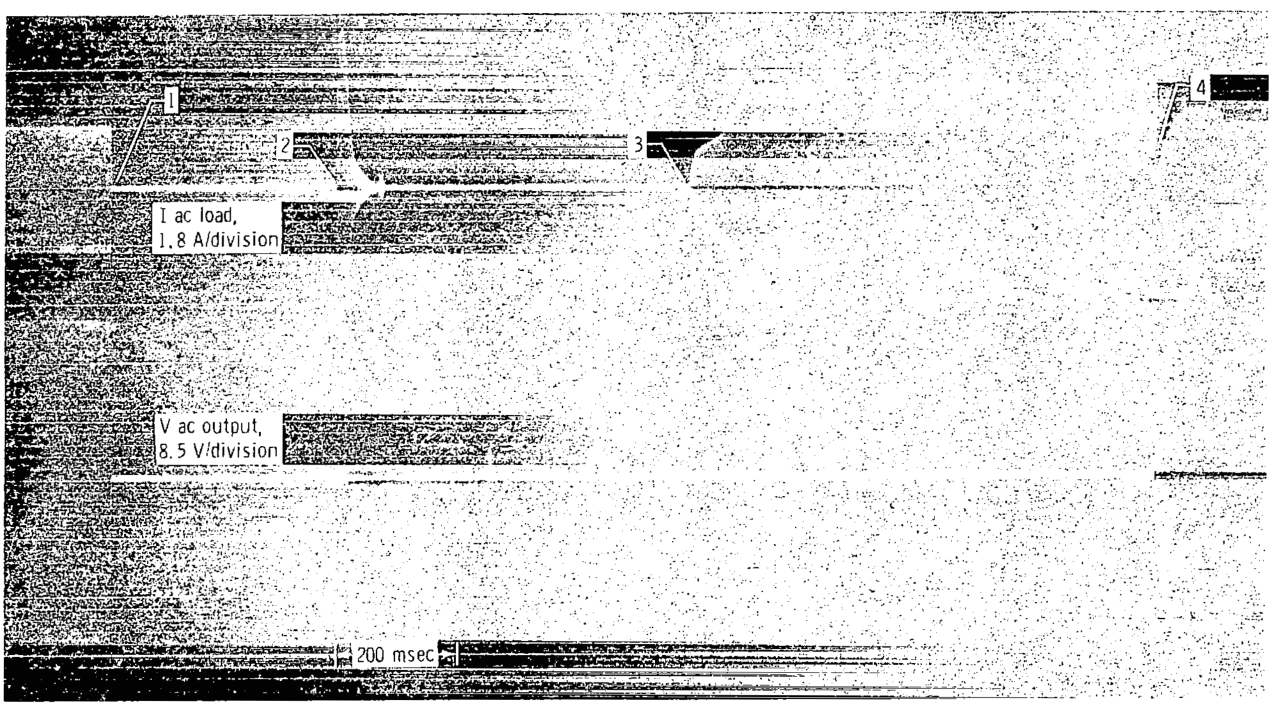



Figure 21. - Short-circuit response of single-phase inverter module.

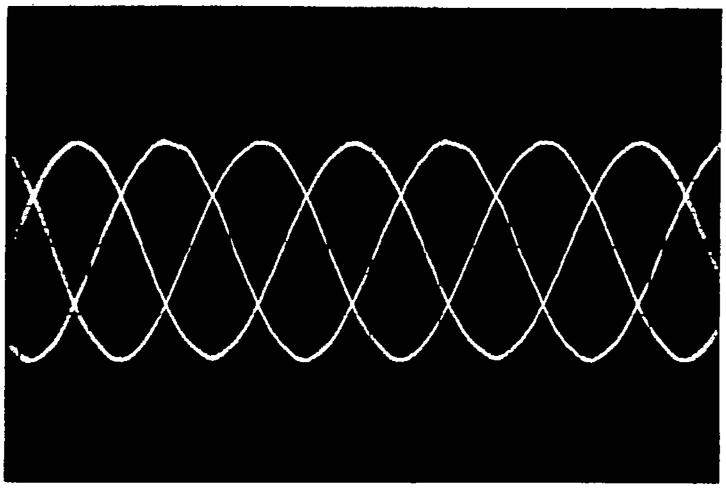


Figure 22. - 400-Hertz, three-phase output voltage of inverter module. Vertical scale, 100 volts per division; horizontal scale, 0.5 millisecond per division.

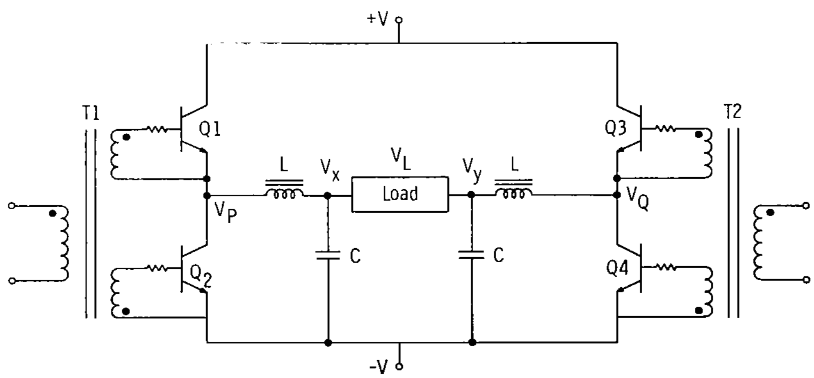
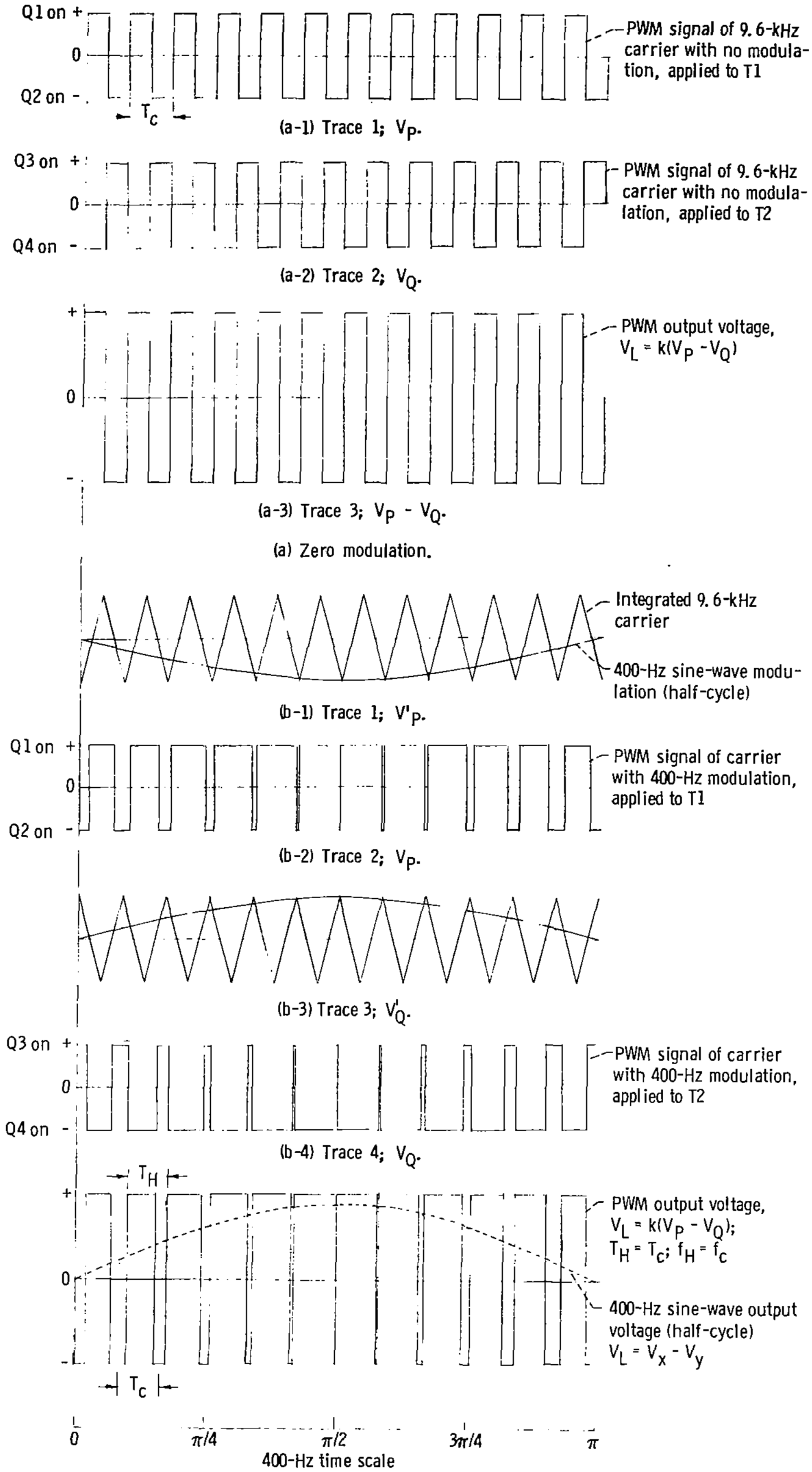


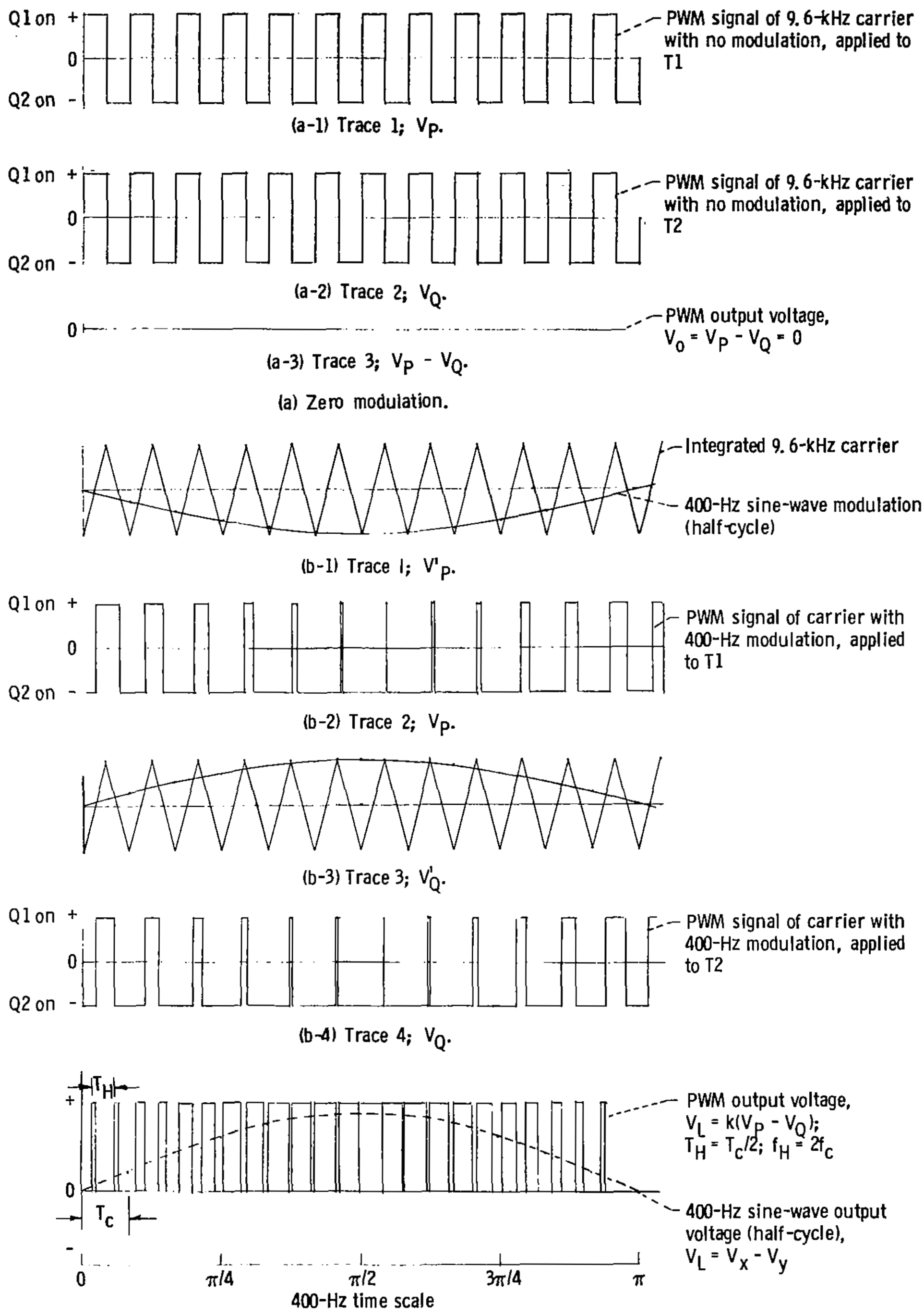

Figure 23. - Single-bridge circuit. $V_P$ and $V_Q$ are square-wave voltages of carrier-frequency and low-frequency modulation; $V_x$ and $V_y$ are average voltages of low-frequency modulation only.




(b-5) Trace 5, $V_P - V_Q$.

(b) Modulation index, ~ 100 percent.

Figure 24. - Conventional pulse width modulation.




(a-1) Trace 1; $V_P$.

(a-2) Trace 2; $V_Q$.

(a-3) Trace 3; $V_P - V_Q$.

(a) Zero modulation.

(b-1) Trace 1; $V'_P$.

(b-2) Trace 2; $V_P$.

(b-3) Trace 3; $V'_Q$.

(b-4) Trace 4; $V_Q$.

(b-5) Trace 5; $V_P - V_Q$.

(b) Modulation, ~ 100 percent.

Figure 25. - Carrier-cancellation pulse width modulation for single-bridge circuit.

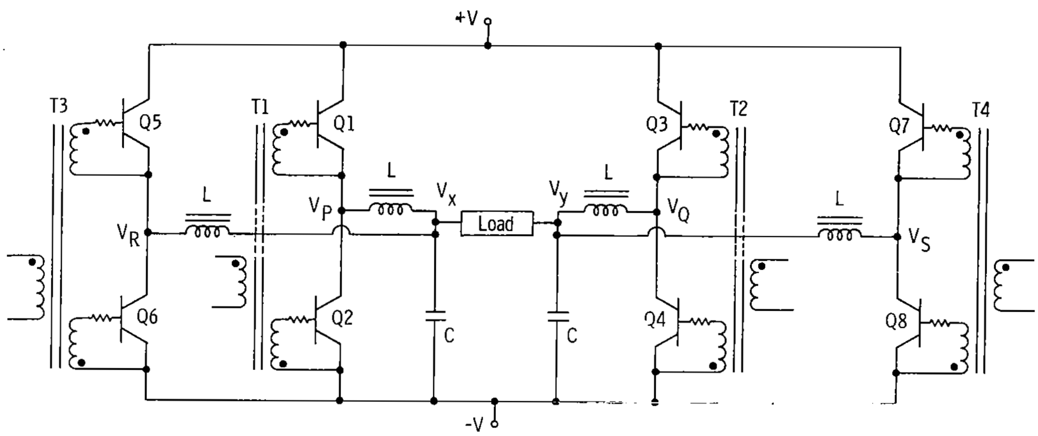
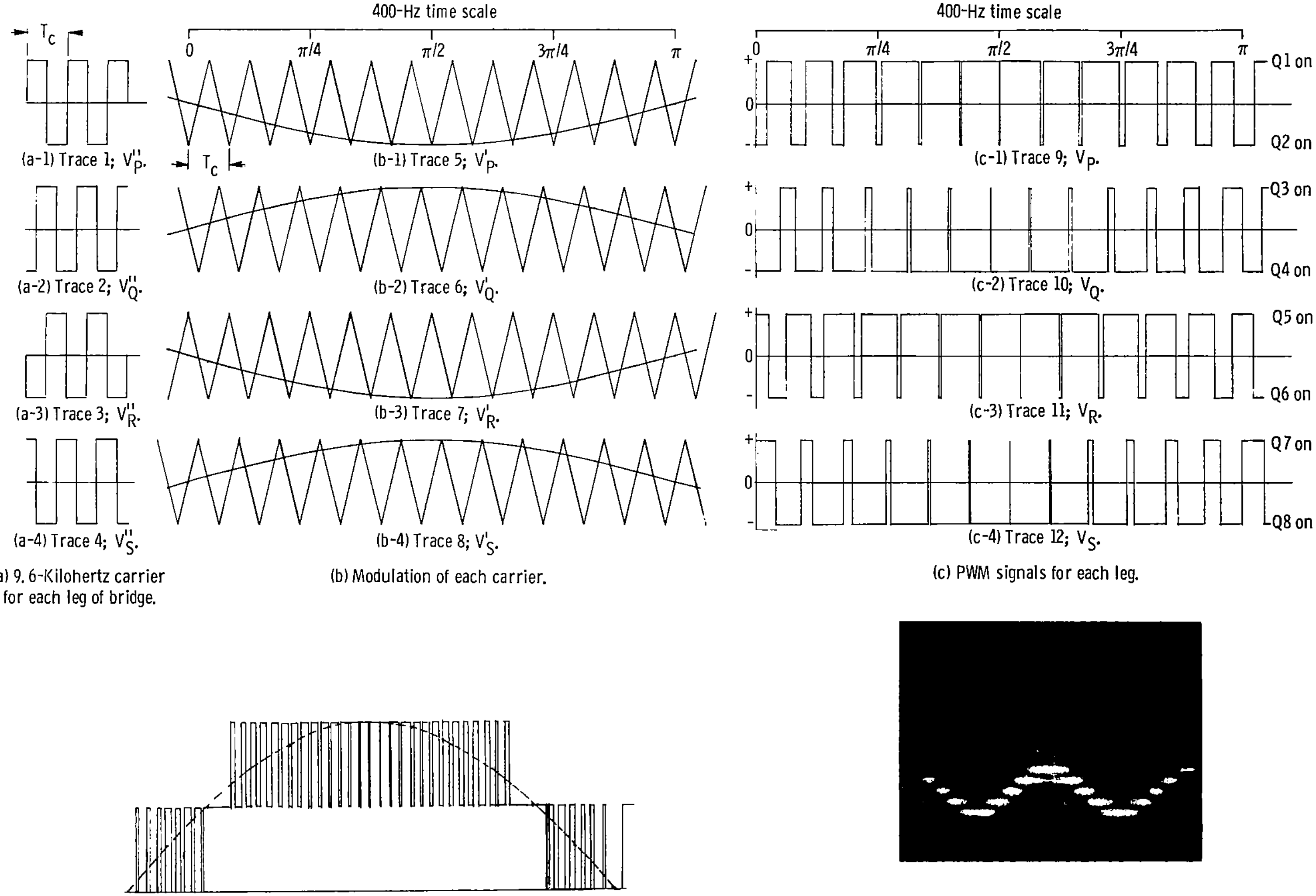



Figure 26. - Double-bridge circuit.




(a-1) Trace 1; $V''_P$.
(a-2) Trace 2; $V''_Q$.
(a-3) Trace 3; $V''_R$.
(a-4) Trace 4; $V''_S$.

(a) 9.6-Kilohertz carrier for each leg of bridge.

(b-1) Trace 5; $V'_P$.
(b-2) Trace 6; $V'_Q$.
(b-3) Trace 7; $V'_R$.
(b-4) Trace 8; $V'_S$.

(b) Modulation of each carrier.

(c-1) Trace 9; $V_P$.
(c-2) Trace 10; $V_Q$.
(c-3) Trace 11; $V_R$.
(c-4) Trace 12; $V_S$.

(c) PWM signals for each leg.

(d) PWM output before filtering ($T_H = T_c/4$; $f_H = 4f_c$). Trace 13; $(V_P + V_R) - (V_Q + V_S)$.

(e) Slope trace obtained by summing the four outputs of the pulse width modulator circuits of the experimental inverter.

Figure 27. - Staggered-phase carrier cancellation. Modulation index, ~100 percent.

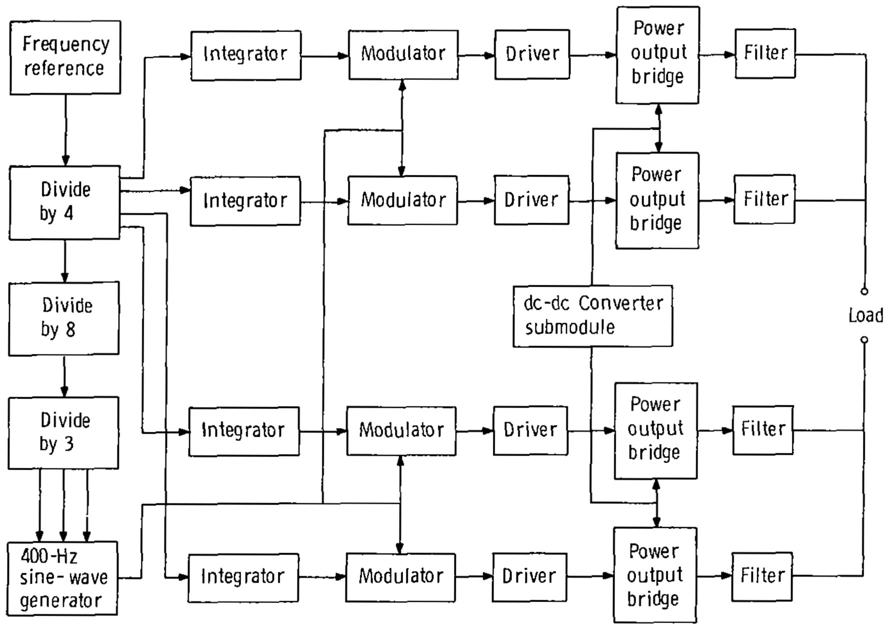



Figure 28. - Block diagram of single-phase dc-to-ac inverter.

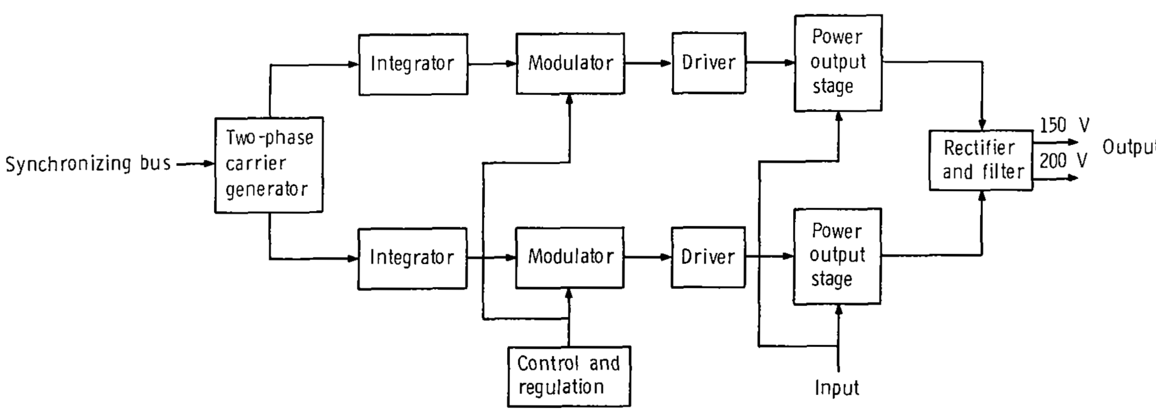



Figure 29. - Block diagram of dc-to-dc converter submodule.

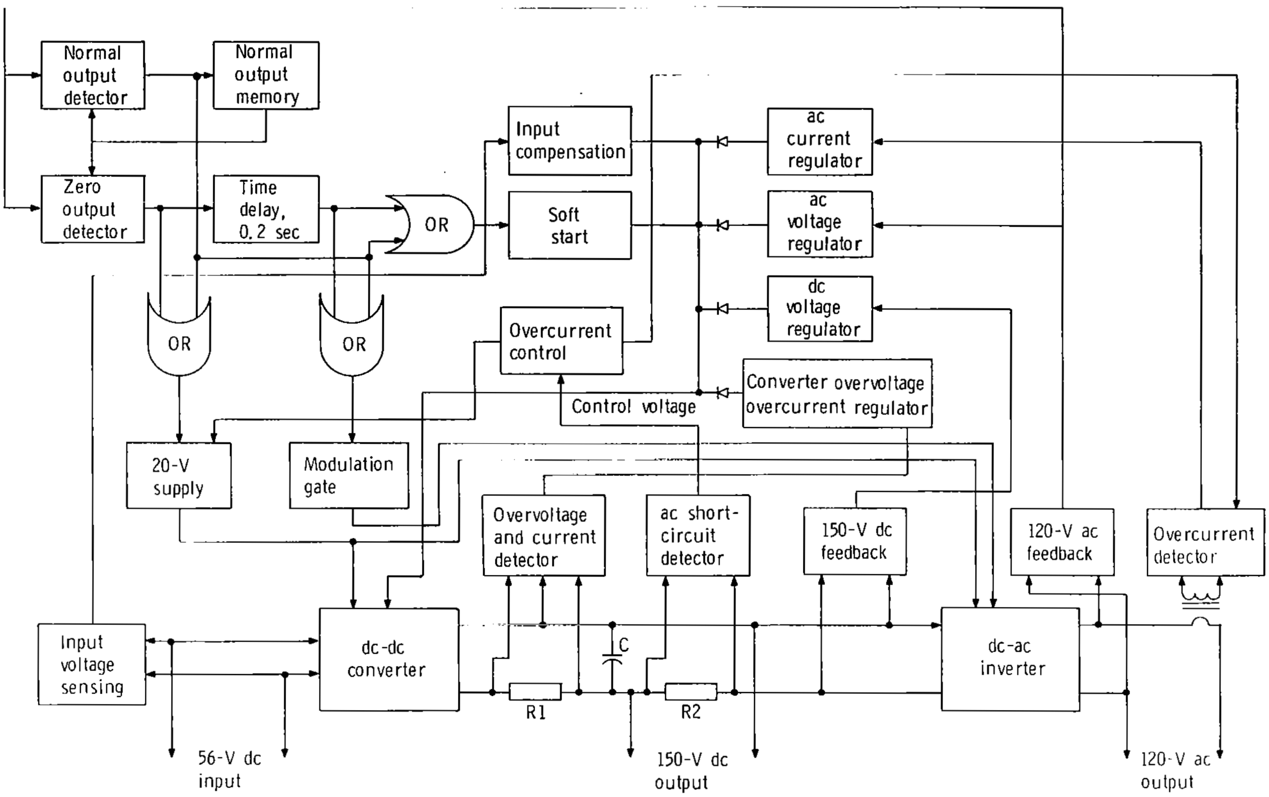



Figure 30. - Block diagram of control and regulation system.

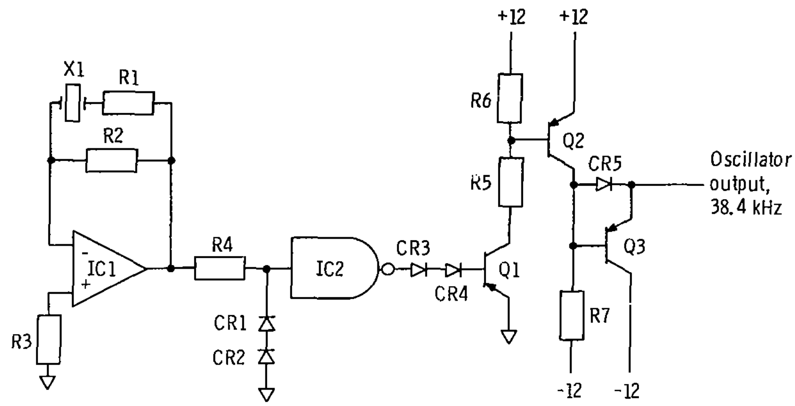



Figure 31. - Frequency reference circuit.

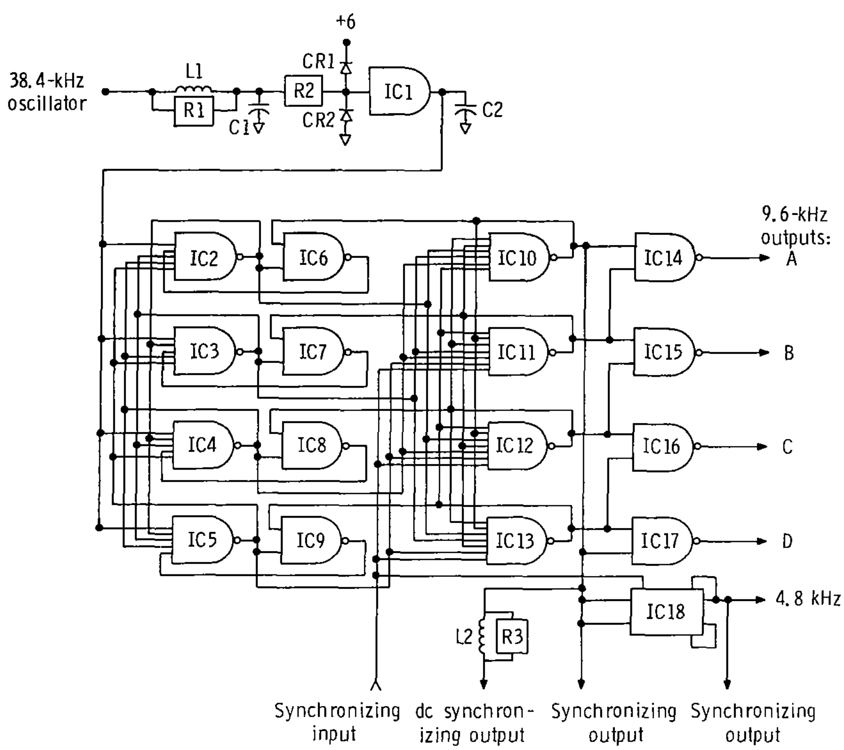



Figure 32. - Countdown circuit.

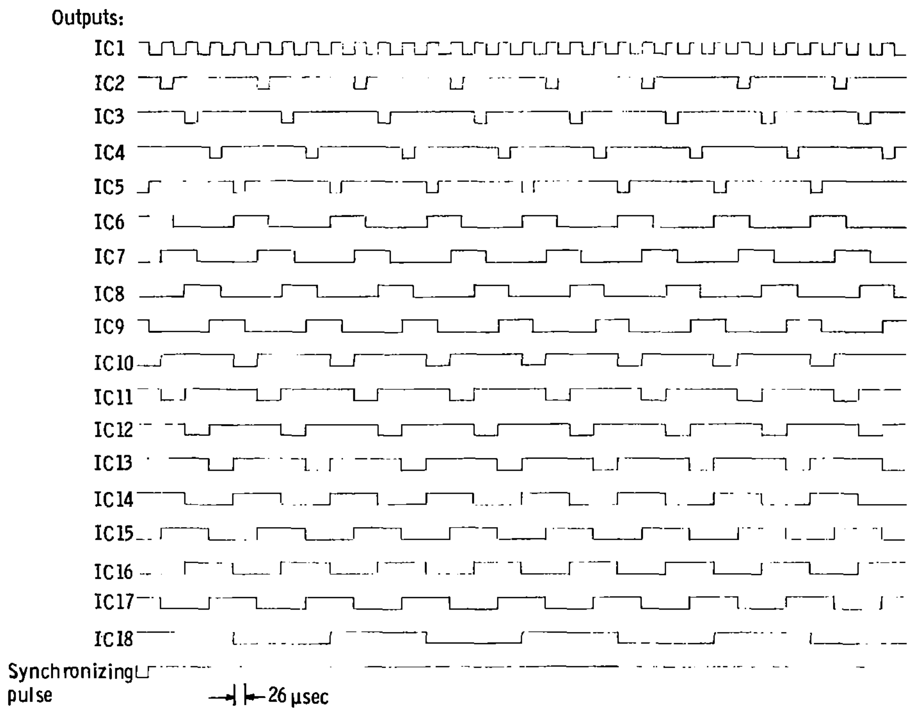



Figure 33. - Timing diagram of countdown circuit.

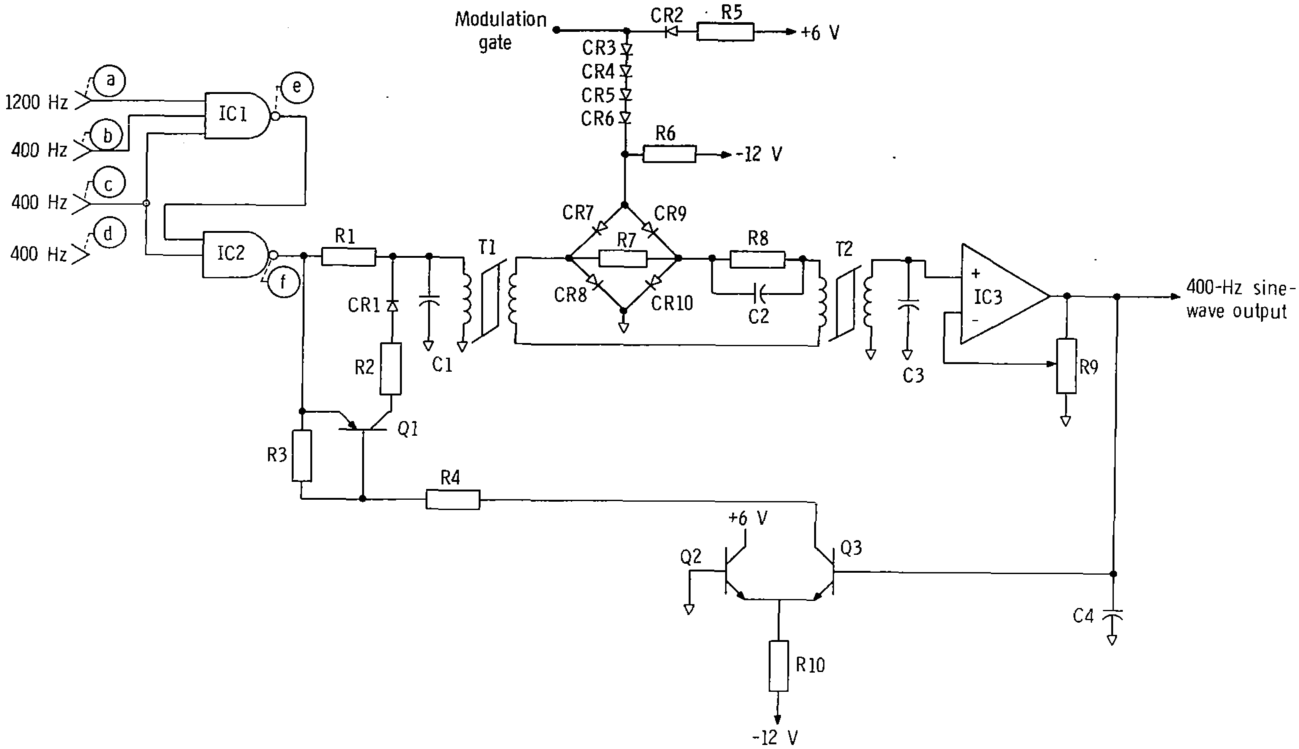



Figure 34. - 400-Hertz sine-wave generator.

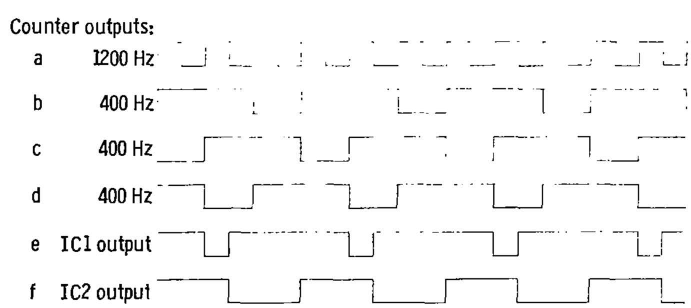



Figure 35. - Timing diagram of 400-hertz square-wave generation.

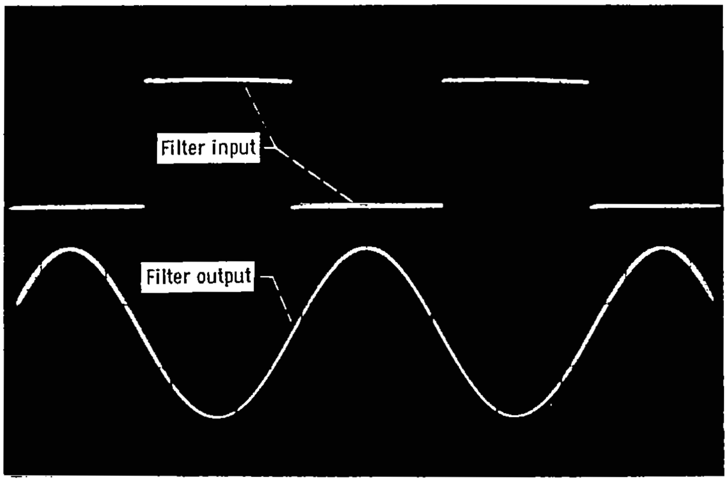



Figure 36. - Formulation of 400-hertz sine-wave modulating signal. Voltage scale, 2 volts per division; time scale, 0.5 millisecond per division.

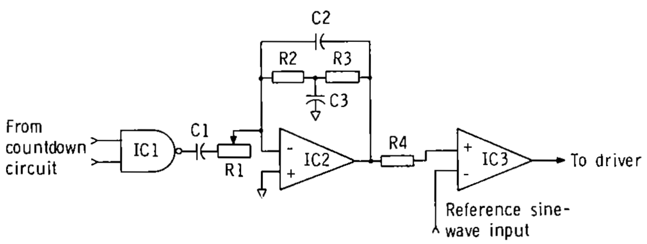



Figure 37. - Carrier generator modulator.

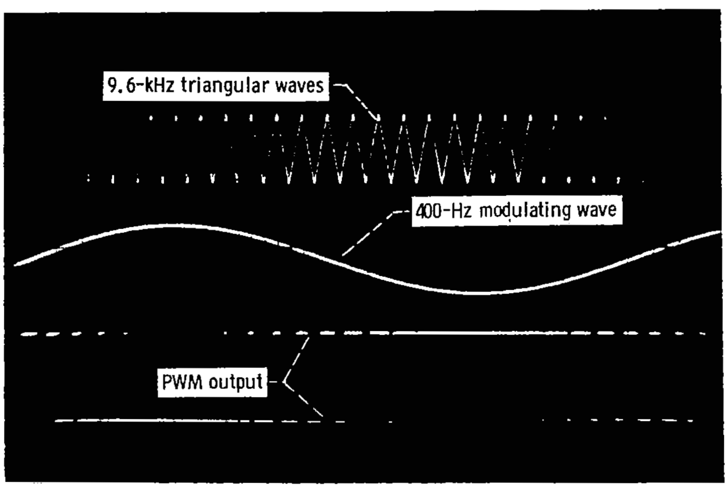
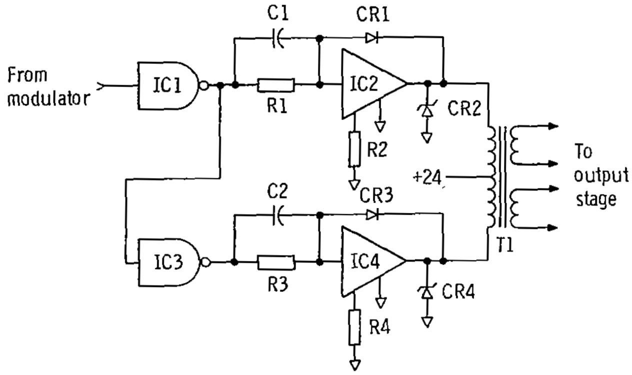
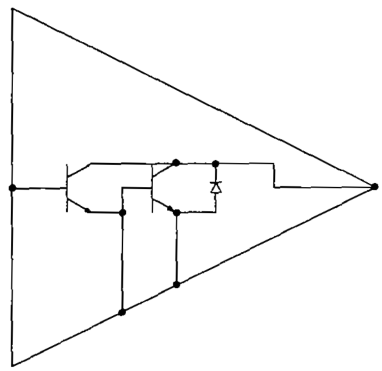



Figure 38. - Formulation of pulse-width-modulated (PWM) signals from triangular and sine wave inputs. Voltage scale, 5 volts per division; time scale, 0.25 millisecond per division.




(a) Driver circuit.



(b) Driver circuit power-integrated circuit.

Figure 39. - Pulse-width-modulated driver circuit.

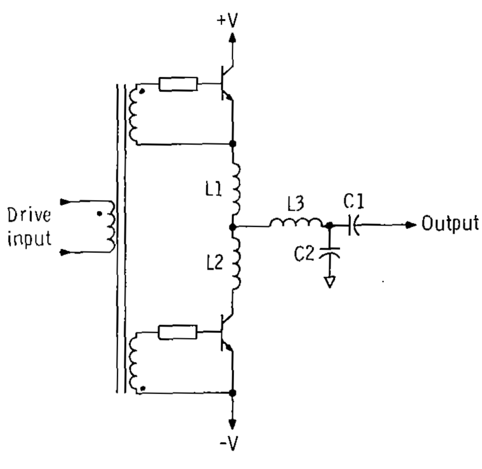



Figure 40. - Simplified ac output stage.

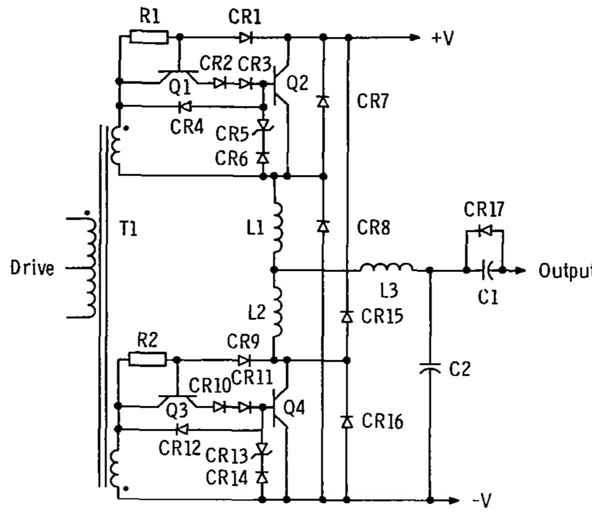



Figure 41. - One leg of inverter output stage and filter.

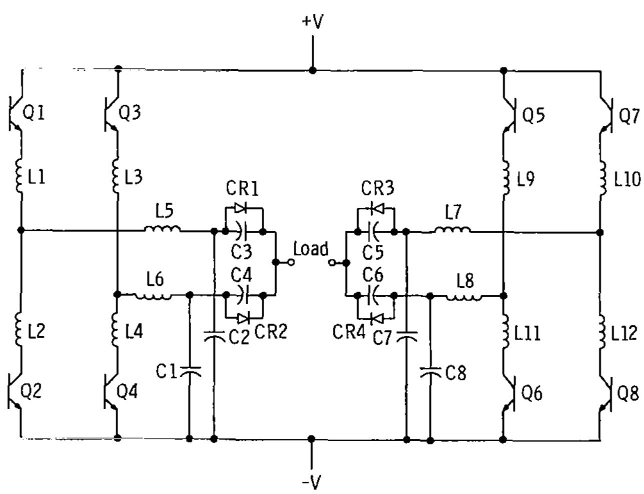



Figure 42. - Inverter output filter.

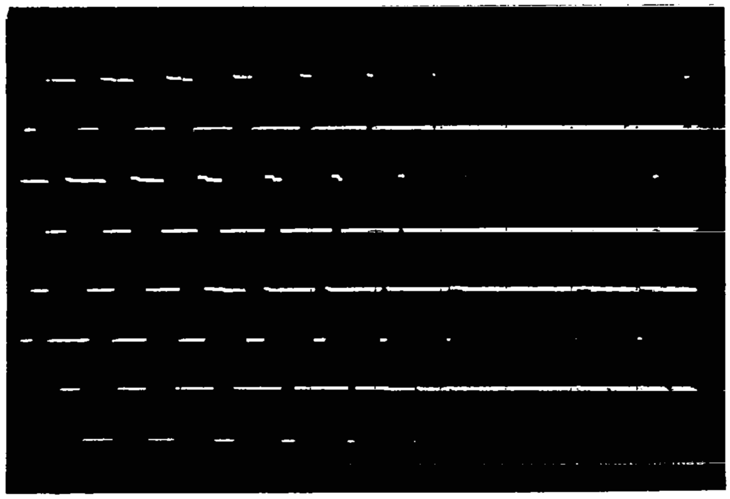


Figure 43. - Collector-emitter output voltages for four transistors in power bridge circuit. Time scale, 0.1 millisecond per division; voltage scale, 200 volts per division.

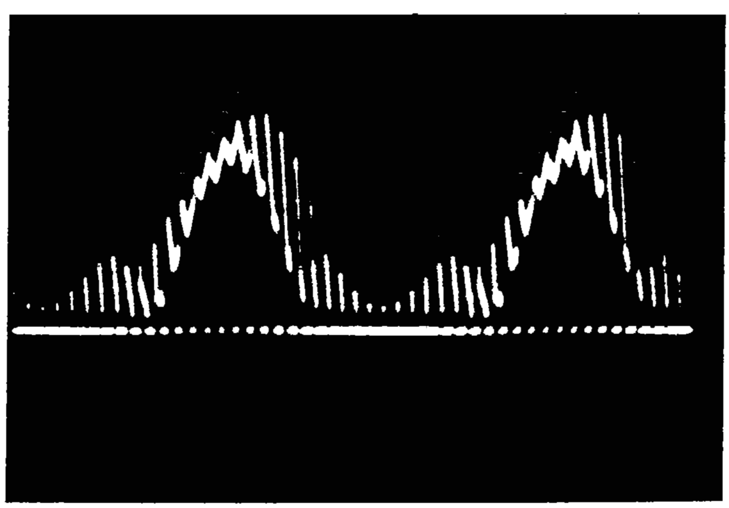


Figure 44. - Collector current of one power transistor in output bridge circuit. Inverter load, 500 watts. Current scale, 1 ampere per division; time scale, 500 microseconds per division.

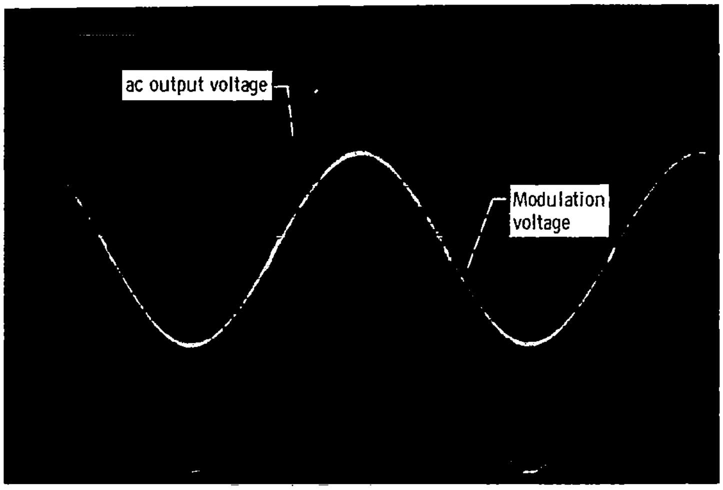



Figure 45. - Comparison of 400-hertz ac output voltage with 400-hertz modulating voltage. Output voltage scale, 50 volts per division; modulation voltage scale, 2 volts per division; time scale, 0.5 millisecond per division.

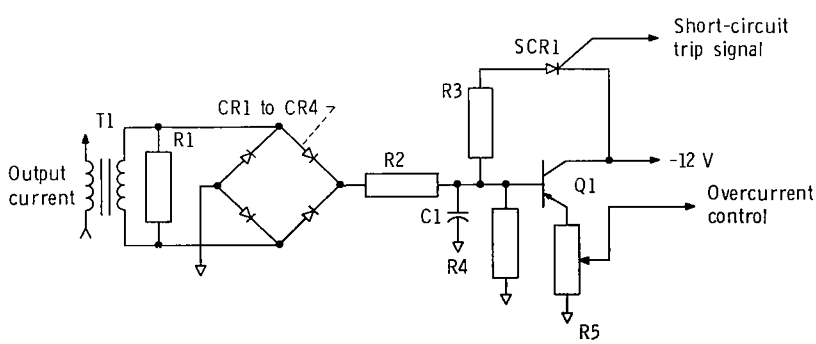



Figure 46. - ac output current sensor.

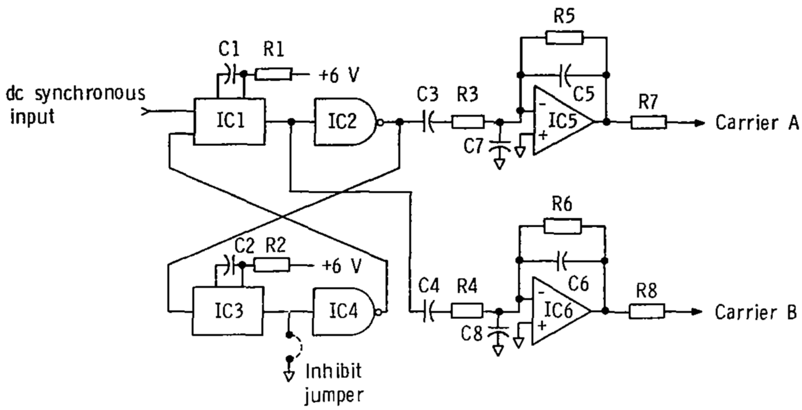



Figure 47. - Converter two-phase carrier generator.

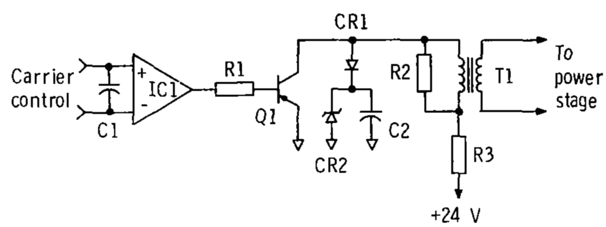



Figure 48. - Converter modulator and driver.

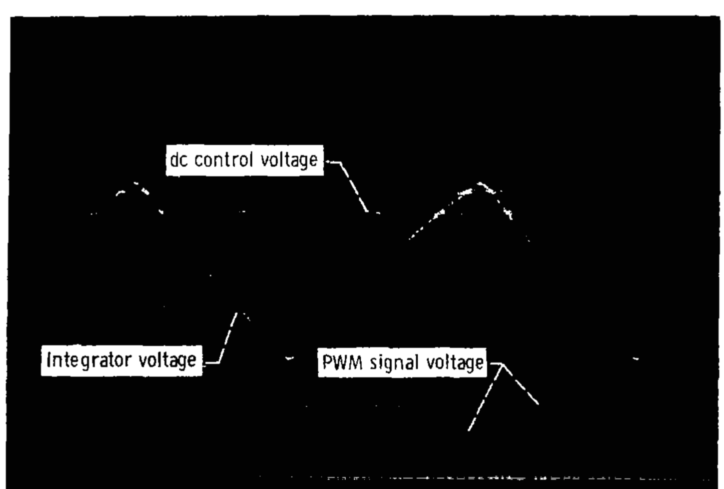



Figure 49. - Pulse-width-modulated (PWM) signal generation for dc-to-dc converter. Integrator voltage scale, 2 volts per division; dc control voltage scale, 2 volts per division; PWM signal voltage scale, 5 volts per division; time scale, 20 microseconds per centimeter.

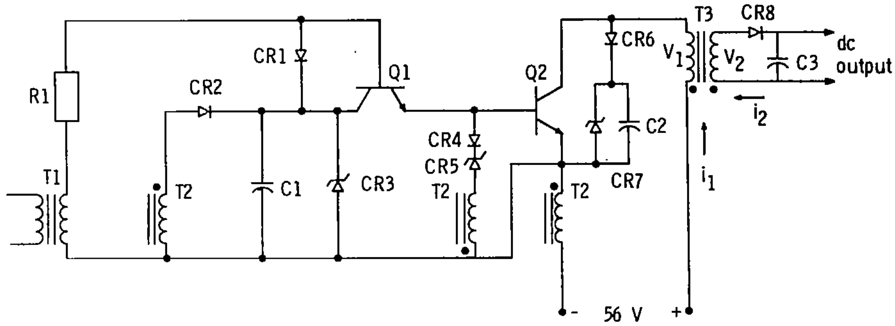
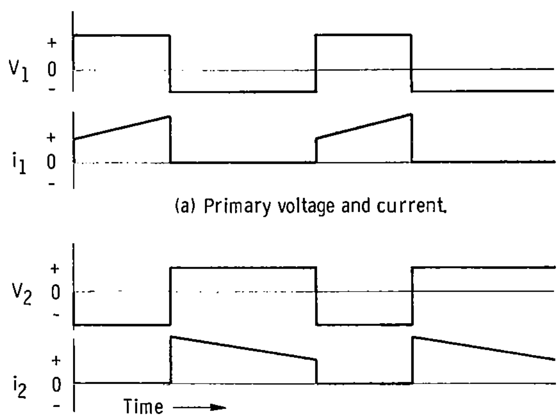



Figure 50. - Converter power stage and driver.




(b) Secondary voltage and current.

Figure 51. - Timing diagram of converter power stage.

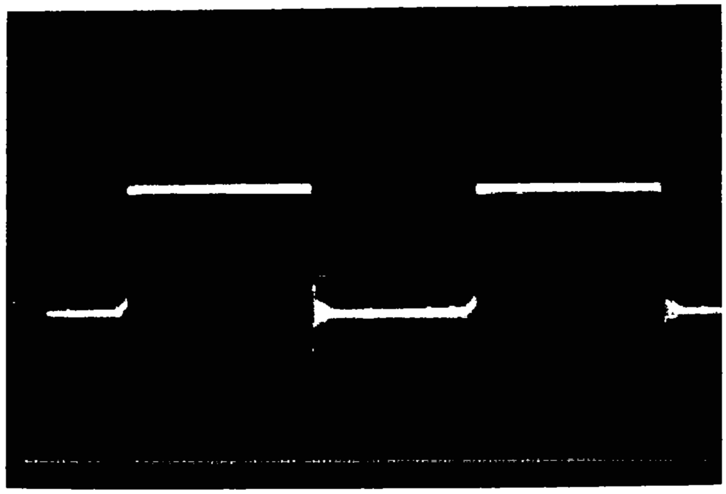


Figure 52. - Transformer output voltage of dc-to-dc converter. Voltage scale, 200 volts per division; time scale, 20 microseconds per division.

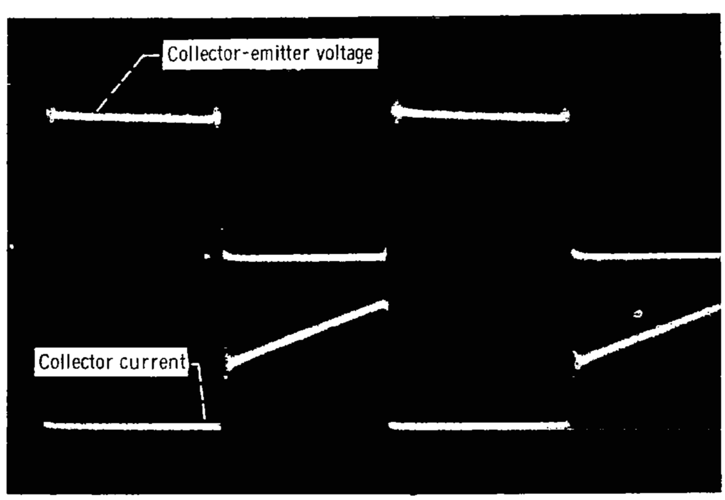



Figure 53. - Collector-emitter voltage and collector current of power transistors in dc-to-dc converter. Load, 500 watts. Collector-emitter voltage scale, 50 volts per division; collector current scale, 10 amperes per division; time scale, 20 microseconds per division.

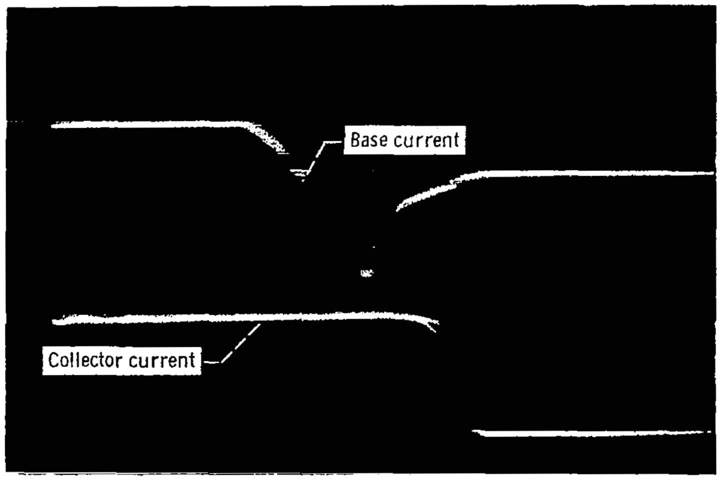



Figure 54. - Base and collector currents of power transistors in dc-to-dc converter during turnoff. Load, 500 watts. Base current scale, 4 amperes per division; collector current scale, 10 amperes per division; time scale, 1 microsecond per division.

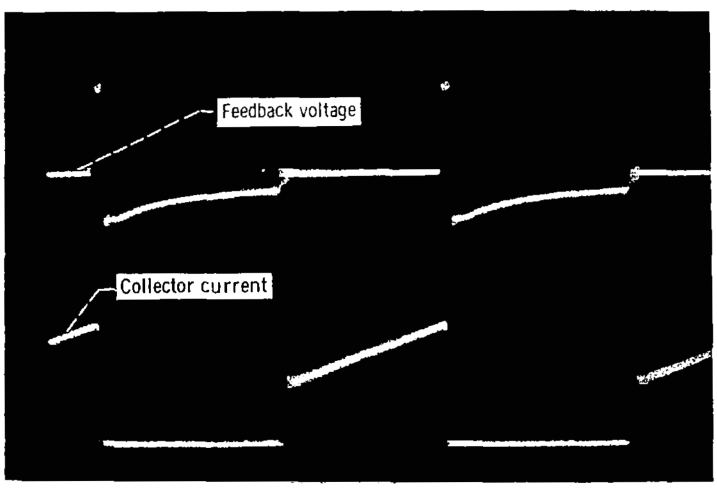



Figure 55. - Feedback transformer voltage and collector current of power transistors in dc-to-dc converter. Feedback voltage scale, 20 volts per division; collector current scale, 10 amperes per division; time scale, 20 microseconds per division.

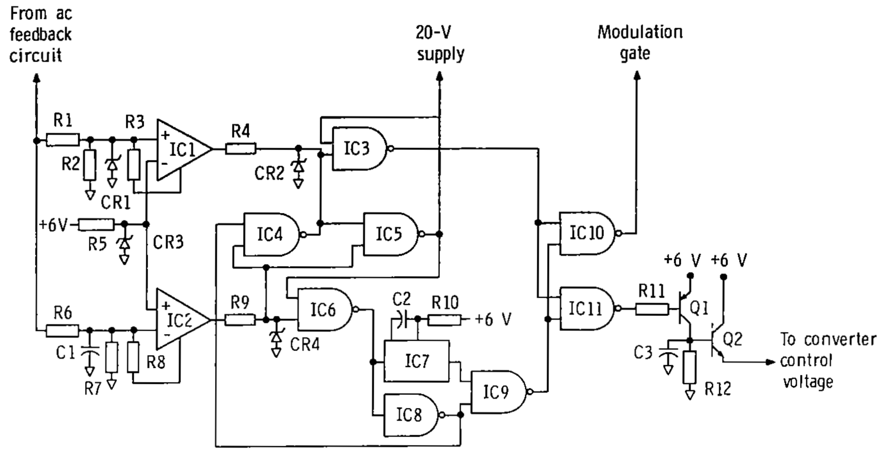



Figure 56. - Startup circuit.

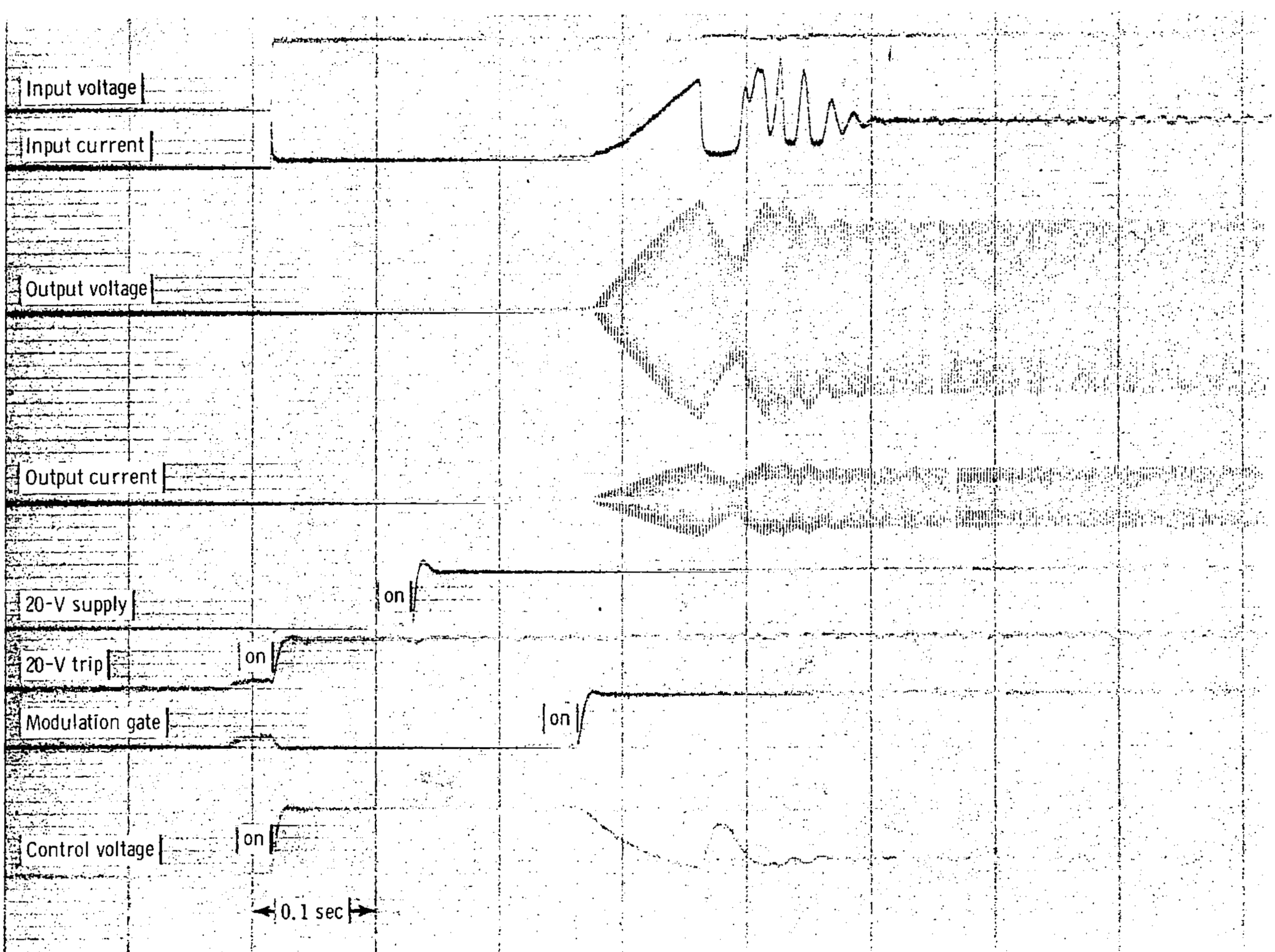



Figure 57. - Inverter turnon sequence.

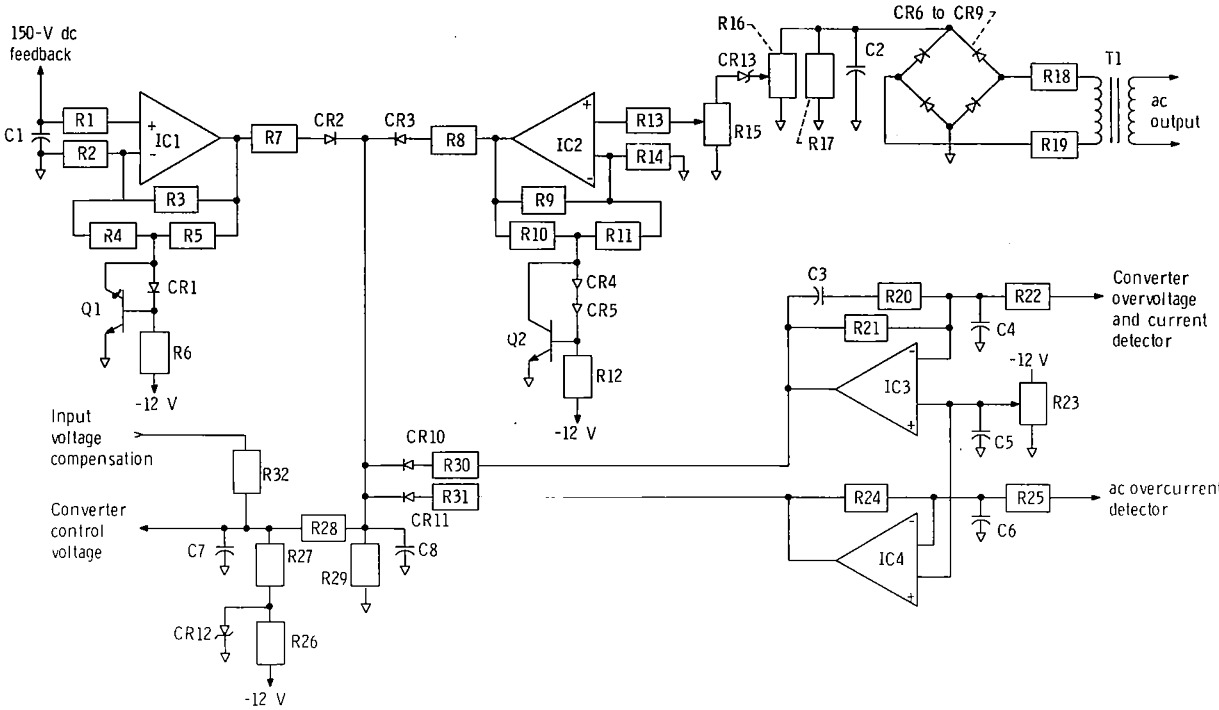



Figure 58. - Converter regulation system.

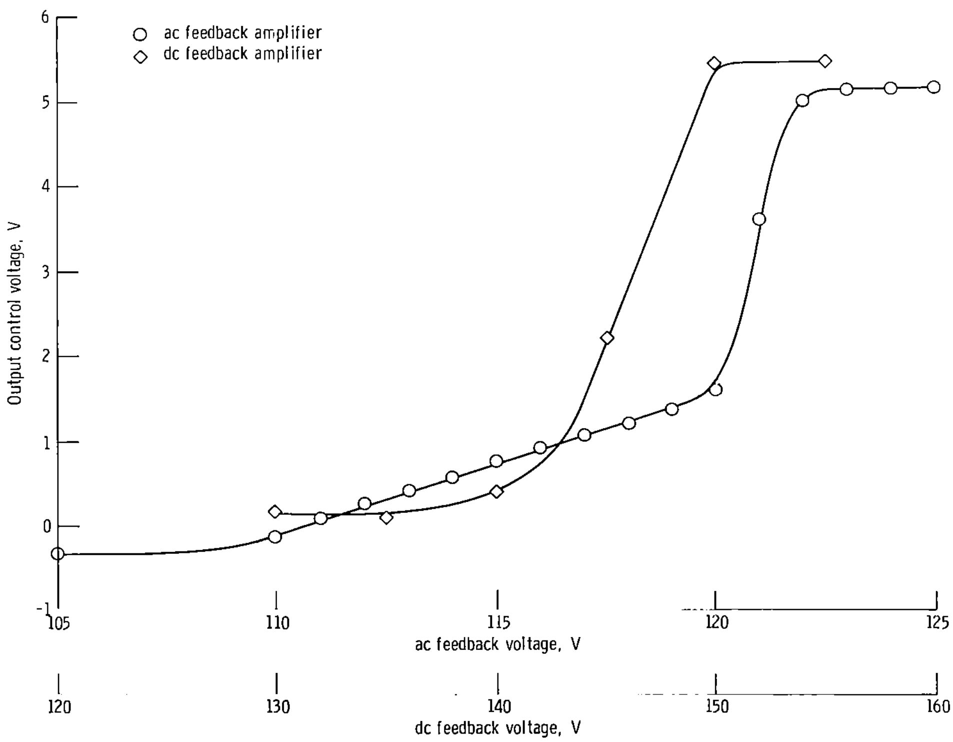



Figure 59. - Transfer characteristic curves of ac and dc feedback amplifiers.

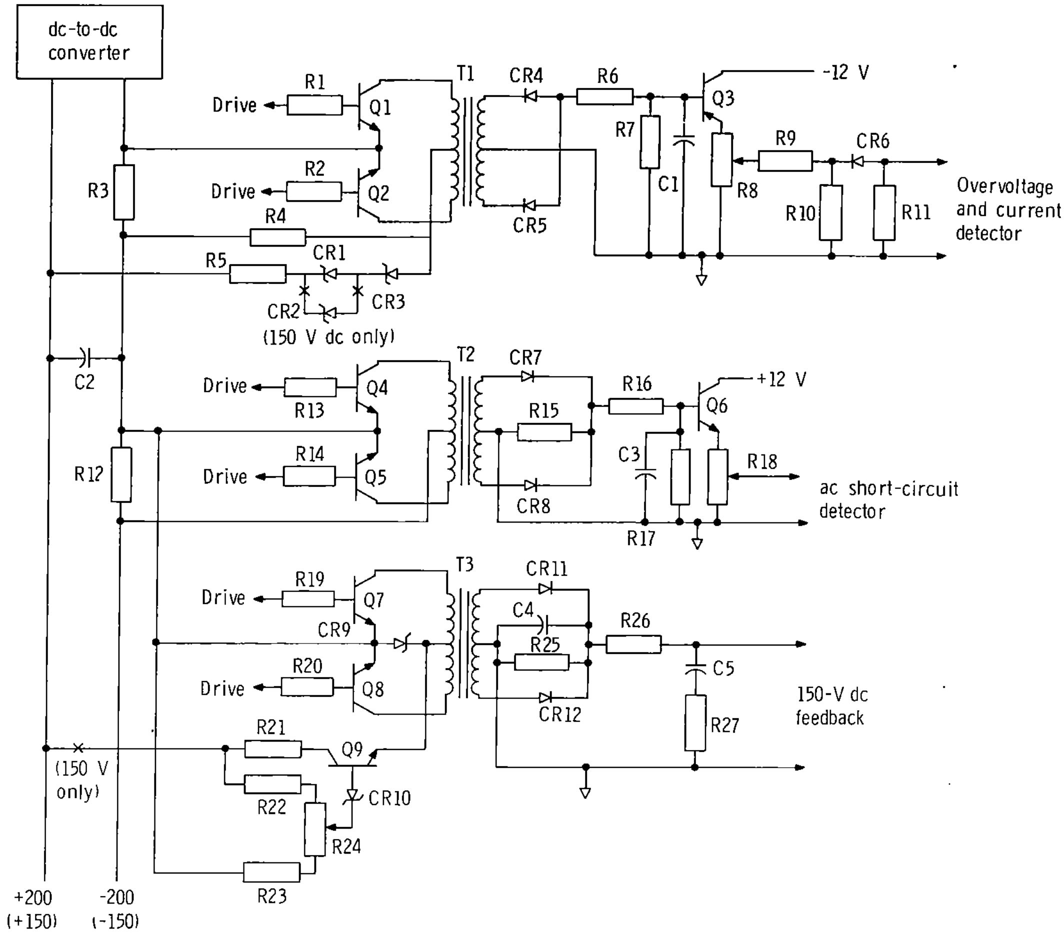



Figure 60. - Converter feedback system.

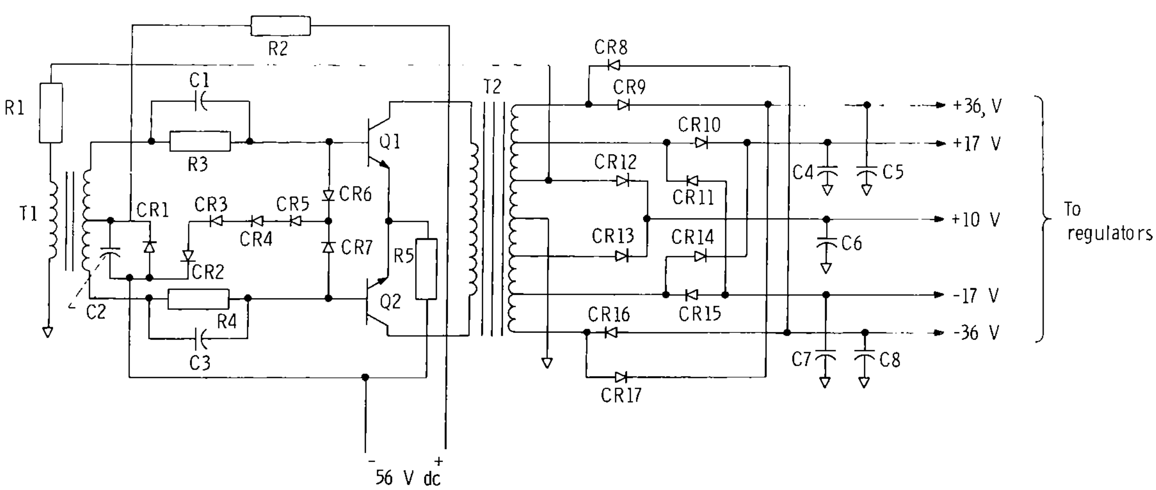



Figure 61. - Low-voltage power supply converter.

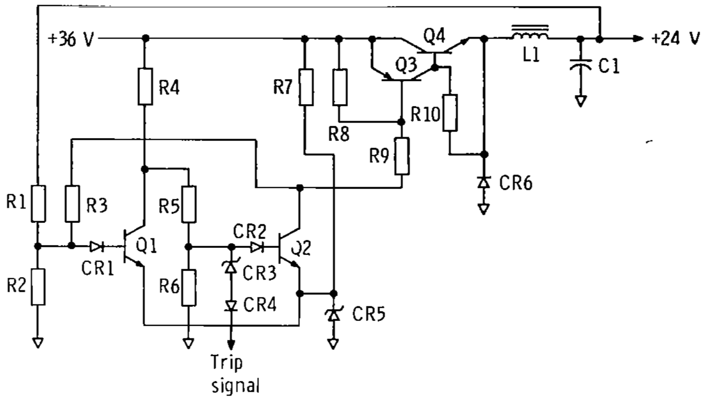



Figure 62. - 28-Volt switching regulator.

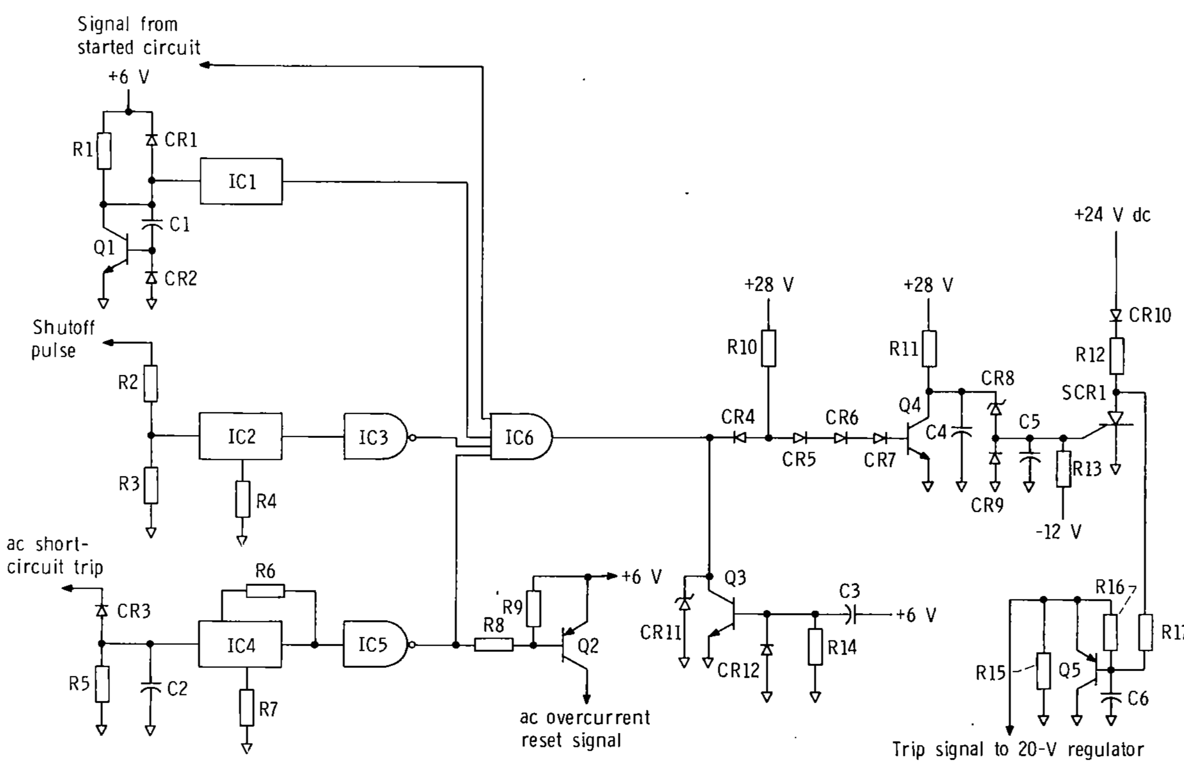



Figure 63. - 20-Volt regulator control circuit.